Pluto

User Manual
Pluto 5 Casino Controller

Document No. 80-15744 Issue 5 HEBER LTD

Current Issue :- Issue 5 - 12th August, 2003

Previous Issues :- Issue 1 - 8th June, 1999
Issue 2 - 4th January, 2000
Issue 3 – 5th February 2002
Issue 4 - 8th October, 2002

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1 INTRODUCTION

The **Pluto 5 Casino Controller** board is a natural progression in the **Pluto** family of products. It builds on the proven reliability and technical excellence of previous **Pluto** boards and provides improved performance and flexibility at lower cost. This manual covers the detail of the hardware operation of **Pluto 5 Casino Controller** board, other boards in the system have their own manuals.

2 NEW IN THIS RELEASE

- Section 7.13 includes information about the Calypso 16 Video Card.
- Section 9.1 includes information about Box Header type connectors and their corresponding part numbers.
- Schematic drawings have been updated to reflect hardware changes.

3 OVERVIEW

The **Pluto 5 Casino Controller** board is a low cost, high performance single board controller for amusement machines. An 8 reel machine with 256 lamps, 32 LED digits, Linewriter display, Coin Acceptors, Note Acceptors and Payout Hoppers can be controlled without any additional boards.

Single channel sound can be played through one or two speakers. Two Channel (mono or stereo) sound is available by plugging in an additional IC.

Pluto 5 Casino boards are supplied with either Ultrex or Box Header connectors.
Pluto 5 Casino with Ultrex connectors is referred to as **Pluto 5CU.**
Pluto 5 Casino with Box Header connectors is referred to as **Pluto 5CB.**
These connectors and all the other connectors on the Pluto 5 Casino board are documented in section 9 - Connector Types and Pin Outs in this user manual.

4 DIFFERENCES FROM PLUTO 5

The Pluto 5 Casino Controller is basically an upgrade to the standard Pluto 5 Controller with the following additional functionality added:

1. Provision for up to 6 extra serial communication ports, Channels3 C-H, by fitting DUARTs U53, U54 & U55.
2. Additional 32Kbyte RAM with independent battery backed supply.
3. Provision for a battery powered PIC Microcontroller which allows power-down monitoring of up to 7 external switches.

To allow the above additions, the following changes have been made to the operation of the controller:

1. A standard Pluto 5 FPGA will not work in the Pluto 5 Casino Controller (the functions of pins 48 & 54 are changed).
2. The Multiplex Expansion (MPX2) facility offered on Pluto 5 has been lost
3. The General Purpose TTL outputs and external I^2C Bus on connectors P12 & P13 have been remapped.

5 CIRCUIT SCHEMATIC DESCRIPTION

This section is a walk through of the **Pluto 5 Casino Controller** board (56-15741) circuit schematics, Figures 1-13 of this document. A detailed description is given in Section 4 “CIRCUIT OPERATION”.

5.1 Sheet 1

This sheet shows the interconnection between the remaining sheets of this drawing.

5.2 Sheet 2

This sheet shows the following items:

- Motorola MC68340 Processor.
- Pull-up resistors on Address Bus, Data Bus and other Control Signals.
- Push Button Switch, SW3.
- P16 “BACKGROUND DEBUG MODE” connector.

5.3 Sheet 3

This sheet shows the FPGA.

5.4 Sheet 4

This sheet shows the following memory related circuits:

- Sockets for 1 or 2 EPROMs, U1 and U2
- 64Kbytes Battery backed RAM, U3 and U4
- P15 “MEMORY EXPANSION” connector for plug-in Memory Cards

5.5 Sheet 5

This sheet shows the following sound related circuits:

- Standard Sound Channel #1, U8 (OKI MSM6585).
- Optional Sound Channel #2, U39 (OKI MSM6585).
- TDA7057AQ Stereo Audio Amplifier.
- P10, “LS” connector for loudspeakers.

5.6 Sheet 6

This sheet shows the 64 Open Drain Outputs, OP0-63.

5.7 Sheet 7

This sheet shows the following circuits:

- External inputs, IP0-31
- Two 8 way DIL switches, SW1 and SW2

5.8 Sheet 8

This sheet shows various Power Supply related functions:

- Current sensing +12V Meter supply
- Power fail detection.
- Current sensing from Lamp Multiplex.
- Fuse and +5V regulator.
- Voltage rail overvoltage and transient protection.
- P3 “PWR IN” power input connector

5.9 Sheet 9

This sheet shows the following I/O connectors.

- P7 “REELS” carries enough I/O lines to run 6 reels, including a sub set of the lamp multiplexer and power supplies for the motors.
- P8 “I/O 1” and P9 “I/O 2” are general purpose I/O.
- P11 “MULTIPLEX EXPANSION” provides signals for the connection of Multiplex Expansion boards.
- P12 “AUX OUTPUTS” provides 6 open drain TTL outputs, typically for driving VFD displays.
- P13 “I^2C” provides a connector for external I^2C expansion, e.g. E^2PROM modules. Note that the lines used to implement this connector are different to the lines allocated for the internal I^2C bus to U40 and U37.
- P14 “I/O EXPANSION” is a position for a daughter board for I/O expansion.

5.10 Sheet 10

This sheet shows the following circuits and connectors:

- Reset circuit and LED.
- Battery Backup for RAM and optional Real Time Clock.
- Optional I^2C Real Time Clock socket, U40, PCF8583.
- Optional I^2C E^2PROM socket, U37, 24C04 (512 bytes) or 24C08 (1024 bytes).
- RS232 buffers.
- P1 “RS232” is a general purpose RS232 serial communication port.
- P2 “DATAPORT” is the BACTA standard Dataport.

5.11 Sheets 11, 12 & 13

These sheets show the Multiplex Lamp and LED drive circuits and connectors.

- Sheet 11 shows the Lamp Columns/Digits Sink drivers.
- Sheet 12 shows the Lamp Row/Source drivers
- Sheet 13 shows the LED Segment drivers
- P4 “LAMP SINKS” is the Lamp Array Column/Sink outputs
- P5 “LED” is the connector for the 32 or 16 LED digits.
- P6 “LAMP SRC” is the Lamp Array Row/Source outputs

5.12 Sheets 14

Sheets 1-13 are identical to the standard Pluto 5 Board. This sheet is a secondary Root Sheet showing the extra 4 schematics (Sheets 15-18) that have been added to make the Pluto 5 Casino.

5.13 Sheets 15

This sheet shows the three 68681 DUARTs (U53-U55) that provide serial comms channels C-H.

5.14 Sheets 16

This sheet shows the following:

- Buffers for the 5 RS232 channels, C-G.
- Connector P17 for RS232 Channel C
- Connector P18 for RS232 Channels D, E, F & G.

5.15 Sheets 17

This sheet shows the Channel H Interface. This is at TTL levels and may connect directly, via P19, to a variety of different format Interface Cards, eg RS422, RS485, Opto-Isolated RS485, etc.

5.16 Sheets 18

This sheet shows the following:

- Optional security PIC Microcontroller, U51.
- Security switch connector, P20.
- Second non-volatile (battery-backed), 32Kbyte RAM, U50.
- Second battery and back-up circuit for U51 and U50

6 CIRCUIT OPERATION

This section describes how some elements of the circuit operate and their capabilities and limitations. A subsequent section deals with how the various capabilities of the board are used to implement specific amusement machine functions.

6.1 Power Supplies

The Power Input to the board is on P3. There are 3 input voltages required, +12V, -12V and 36V or 48V for the lamp multiplex.

The +12V supply is fused by F1 (3.15A) as it comes on the board. From the unfused (input) side, the +12V is distributed to the Reel Connector, P7 where it may be used to provide the supply for the Stepper Motors.

From the fused side, the +12V is used for the following:

- Regulated via U15 to provide the Vcc (+5V) supply for the board. This will draw up to 250mA from the +12V rail.
- To provide the Power Supply for the Stereo Audio Amplifier, U32. The load current drawn by this will depend on the audio volume, etc. but is not likely to exceed an average of about 200mA.
- Monitored by U16B to detect imminent failure of the +5V supply and cause a Level 7 (Non-Maskable) Interrupt, NMI-. The interrupt will occur if the +12V supply drops below approximately 7.8V.
- To provide the Power Supply for the multiplexed LED drive circuits. With 32 LED digits fitted and all having all segments illuminated, the current drain is likely to be between 400mA and 550mA.
- Distributed to various connectors, P1, P2, P8, P9, P12 and P14 for optional use by external circuits.

When connecting external loads to the Fused +12V outputs on P1, P2, P8, P9, P12 and P14 make sure that the total current drawn is within the rating of fuse F1 (3.15A), making due allowances for the other loads as described above.

The –12V supply input provides the negative supply for the 1488 RS232 Transmitter Buffers, U33, U41, U43 & U46, and the –12V supply required on the DATAPORT Connector, P2.

The Lamp Multiplex supply should be +36V or +48V, depending upon the duty cycle employed by the software. See Section 6.15, “Multiplexer” for more information.

Transient suppressers (Tranzorbs) are fitted on the +12V supply (fused side), -12V supply and Vcc to protect these lines against any overvoltage.

6.2 Reset and Power Fail Detection

TL7705 device, U17, on Schematic Sheet 10, provides the system reset. At power up, the system is held in a reset state (RESET- low, RESET high) for about 5 seconds. This time is determined by C14. The processor may initiate a full hardware reset at any time by asserting Port B, pin 0 (PB0) low, which will trigger the TL7705 via the RESIN- pin. The RESET lines will also be immediately asserted by the TL7705 if the Vcc line drops below 4.75V.

While the system is in a reset state, i.e. RESET- is low, a red LED, LD1, is illuminated.

The power fail detection is a simple threshold detection on the 12V rail using one section of the quad comparator LM339 (U16B) on Schematic Sheet 9.

When the +12V input falls below a threshold of approximately 7.8V, the output of the comparator goes low which causes a Level 7 interrupt (NMI) to the processor. This will occur BEFORE the 7805 regulator drops out of regulation and the Vcc line starts to drop, thus giving the processor a period of time to react before the RESET is asserted by the TL7705, U17. The main purpose of giving the

processor the NMI in advance of the RESET is to avoid the risk of an incomplete RAM write operation occurring if the RESET were to be asynchronously asserted while such an operation was being carried out.

The time available between the assertion of NMI and the assertion of RESET will depend on the rate of fall of the +12V line, which will obviously be dependent upon the power supply and the loading on the +12V, but will typically be several milliseconds.

6.3 Primary Battery Backup

A backup battery, BT1, is provided (Schematic Sheet 10) to allow the two RAMs U3 and U4 to retain data while the board is powered down and to keep the optional Real Time Clock chip, U40, running.

BT1 is a two cell rechargeable NiMH (Nickel Metal Hydride) battery, capacity 70mA/hr. The circuit comprising BT1, Q2, R43 and R132 provides the battery trickle charge and switchover of the secured power supply rail, Vbatt.

While Vcc is at 5V, current flows through the base-emitter junction of Q2 through R43 into the battery. On charge, the voltage on BT1 will be about 2.6V so the current through R43 will be $(5-V_{BE}-2.6)/3300$, about 0.5mA. Thus Q2 will be turned ON and Vbatt will be a V_{CEsat} below Vcc. Current will therefore also flow through R132 into Vbatt, $(5-V_{CEsat}-2.6)/3300$, about 0.7mA. Total trickle charge current is therefore 0.5 + 0.7 = 1.2mA. The specification of the cells calls for a trickle charge of between .01C and .03C. C is 70mA, so the acceptable range is between .7mA and 2.1mA.

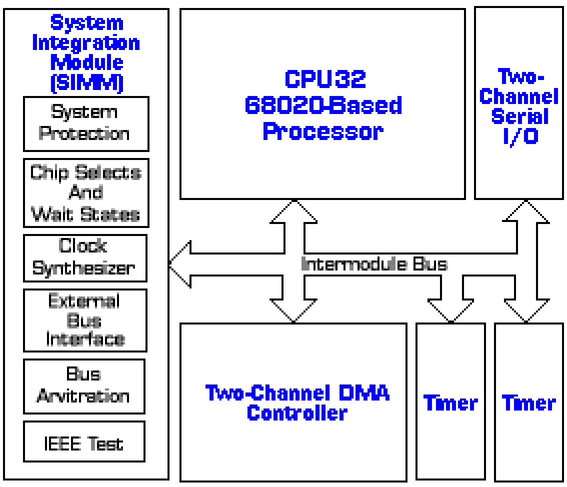
When power is removed, Vcc collapses to ground. The base-emitter junction of Q2 is now reverse biased and therefore no current flows through R43 and Q2 is OFF. Vbatt is now connected to the positive end of BT1 via R132. The discharge current into the RAMs and RTC should not exceed 40µA, which will result in a voltage drop in R132 of less than 0.15V. This gives a worst case battery life in excess of two months, and in practice much higher.

When on battery backup it is vital that the RAMs are placed in the standby state by ensuring that the CS- line is high. Q1 and R42 achieve this. When the RESET- line goes low, which may occur either as a result of a Reset occurring or Vcc collapsing, Q1 turns OFF causing the CS- lines to the RAMs to be pulled to Vbatt by R42.

6.4 The MC68340 Processor

Full details of the operation of the processor is given in the **Motorola MC68340 User Manual** [see Adobe Acrobat File 68340um.pdf, plus Addenda files 68340um_ad.pdf and 68340um_ad2.pdf]

The MC68340 contains the following functional blocks:



6.4.1 CPU32 Processor Module

The CPU32 is a processing core which is basically 68000 code compatible but with a number of enhancements. For full details of operation please refer to both the **Motorola MC68340 User Manual** and the **Motorola M68000 Family Programmers Reference Manual** [see Adobe Acrobat File 68kprm.pdf].

All modern 68000 Compilers and Assemblers have various options for the target CPU. When generating code for the Pluto System, the CPU32 option should be used.

If the Compiler/Assembler is old it is possible that it may not have a CPU32 option. In this case, the Compiler (if used) should be run with the 68000 option set. The assembler may be run in 68020 mode which will allow the use of the MOVES command which is required during initialisation to set up the Module Base Address Register (MBAR) in the MC68340. Care must be taken not to write code that calls any other 68020 instructions that may not be implemented on the CPU32.

The Pluto 5 Development Kit includes a suitable C Compiler and Assembler.

6.4.2 SIM40 System Integration Module

This module controls various aspects of the operation of the processor, such as configuration, clock, external bus, etc.

When used in the Pluto System, the main considerations in the use of this module are:

6.4.2.1 Module Base Address Register

Set the Module Base Address Register, MBAR, to a suitable address during initialisation. This sets the base address of all the internal module registers. In the example code it is set in Module “except.asm” to value 0xffff f000. There is nothing magic about this value, but obviously it must be set to an address that is clear of any other devices in the processor memory map. This register must be set before any other module initialisation is attempted.

6.4.2.2 Chip Selects

Set-up the 4 Chip Select outputs, CS0- to CS3-. The Pluto 5 System allocates these as follows:

CS0 - is used to map the system programme memory. This consists of any EPROM fitted to the on-board EPROM sockets, U1 and U2 plus any extra EPROM or FLASH devices fitted to the Memory Expansion Connector, P14. Exact mapping, within the area defined by CS0-, is carried out be the system FPGA.

CS1 - is used to map the on-board, battery backed RAM and, if fitted, any external RAM on a memory card on connector P15.

CS2 - is used to map both the internal registers of the FPGA and the on-board I/O,

CS3 - is normally spare and is available on the I/O expansion connector, P14. Its main use is for the selection of the optional add-on CGA/VGA Video Card.

After hardware reset, CS0- will be asserted for memory accesses anywhere in the memory map which allows the processor to boot. However, the chip selects must be programmed immediately after Reset and prior to any function or subroutine calls, because until they are, CS1- will not be active and therefore it will not be possible for the processor to access RAM.

Example code for setting up the 4 pairs of Chip Select Base and Mask registers is given in Module except.asm

6.4.2.3 Periodic Interrupt Timer

The “sim40_m.c” Module in the Sample Software sets this timer to provide a high priority 1mS interrupt which is normally used by the software to provide basic system timing. This function is controlled by the PICR and the PITR.

6.4.2.4 Clock Synthesiser Control

The SYNCR controls the operation of the main processor clock. The MC68340 is provided with a 32.768KHz reference to which the main clock is phase locked. After reset, the main clock defaults to 8.39MHz. The maximum clock frequency of the standard MC68340 is 16.77MHz.

6.4.2.5 System Protection

The SYPCR controls the bus monitors and software watchdog. Other safeguards in the design give adequate protection against programme malfunction as a result of noise, etc. The Software Watchdog feature is disabled, however, it could be used if required.

The Bus Monitor should be enabled and may be left set at its default of 64 clock cycles time-out.

6.4.2.6 SIM40 Module Pin Allocations

Pins under the control of the SIM40 module are allocated as follows.

Table 1. Allocation of MC68340 Pins Controlled by SIM40 Module

NAME	PIN	I/O	FUNCTION
PA0/A24-	123	O	To I/O Expansion Connector P14, Pin b1, 3K3 pull-up & RESET to Sound Channel #1, U8
PA1/A25/IACK1-	122	O	To I/O Expansion Connector P14, Pin b2, 3K3 pull-up & RESET to Sound Channel #2, U39
PA2/A26/IACK2-	121	O	To I/O Expansion Connector P14, Pin b3, 3K3 pull-up & Drive for Indicator LED LD2
PA3/A27/IACK3-	120	I	To I/O Expansion Connector P14, Pin b4, 3K3 pull-up & Push Button SW3 Input
PA4/A28/IACK4-	117	I/O	To I/O Expansion Connector P14, Pin b5, 3K3 pull-up & SCL line (I^2C) to RTC, U40 and E^2PROM, U37
PA5/A29/IACK5-	116	I/O	To I/O Expansion Connector P14, Pin b6, 3K3 pull-up & SDA line (I^2C) to RTC, U40 and E^2PROM, U37
PA6/A30/IACK6-	115	I/O	Drives S1 pin on SFX Channel #2 (U39) 3K3 pull-up & MPX Lamp Current Sense Input
PA7/A31/IACK7-	114	I/O	Drives S2 pin on SFX Channel #2 (U39) 3K3 pull-up & MPX Lamp Short Circuit Sense Input
PB0/MODCK	87	O	Drive LOW to initiate hardware reset.
PB1/IRQ1-/CS1-	2	O	CS1- Maps RAM
PB2/IRQ2-/CS2-	3	O	CS2- Maps FPGA registers and I/O
PB3/IRQ3-	4	I	Vmeter current sense input.
PB4/IRQ4-/CS3-	5	I/O	To I/O Expansion Connector P14, Pin a3
PB5/IRQ5-	8	I/O	To I/O Expansion Connector P14, Pin b15, 3K3 pull-up
PB6/IRQ6-	9	I/O	To I/O Expansion Connector P14, Pin b16, 3K3 pull-up
PB7/IRQ7-	10	I	IRQ7-/NMI input from Power Fail Detection Circuit
CS0-/AVEC-	1	O	CS0- Maps ROM, both on-board U1/U2 and on Memory Expansion Connector (via FPGA).

6.4.3 DMA Controller Module

The DMA Module provides 2 DMA Channels. On the Pluto 5 these are used for sending sound data from the Programme Memory to the OKI MSM6585 Sound Chip(s). DMA Channel 1 is used to send data to Sound Channel #1, which is fitted as standard to the Pluto 5 Board. DMA Channel 2 is used for the optional add-on Sound Channel #2 if fitted (IC39).

The DMA channel should be set to work in following modes:

- External request
- Dual address
- Source address incrementing (Memory)
- Destination address not incrementing (FPGA sound register)
- Transfer size = byte
- Interrupt on completion

Pins controlled by the DMA module are allocated as follows:

Table 2. Allocation of MC68340 Pins Controlled by DMA Module

PIN	NO.	I/O	FUNCTION
DREQ1-	16	I	SFX Channel 1 DMA request
DACK1-	15	O	No connection
DONE1-	14	IO	Not used, 3K3 pull-up
DREQ2-	13	I	SFX Channel 2 DMA request
DACK2-	12	O	No connection
DONE2-	11	IO	Not used, 3K3 pull-up

6.4.4 Serial Module

The Serial Module provides Asynchronous Comms on 2 Channels, Channel A and Channel B. It is functionally very similar to the 1681/68681 range of DUARTs.

Channel A is buffered to RS232 levels and connected to connector P1. Signals RX, TX, RTS and CTS are provided.

Channel B is buffered to RS232 levels and connected to DATAPORT connector P2. Signals RX, TX, RTS and CTS are provided.

The 4 Channel A signals are also made available on the TTL Expansion Connector, P14, at TTL levels. Thus, alternative interfaces may be provided on an Add-on Board to allow, say, RS485 or Mars HII interfaces to be implemented.

The exact set up of the Serial Module will obviously depend upon the functionality required.

Pins controlled by the Serial module are allocated as follows:

Table 3. Allocation of MC68340 Pins Controlled by Serial Module

PIN	NO.	I/O	FUNCTION
RXDA	33	I	RX DATA Channel A, P1, Pin 2 (RS232 level) & To IO Expansion Connector P14, Pin c9 (TTL level)
TXDA	32	O	TX DATA Channel A, P1, Pin 3 (RS232 level) & To IO Expansion Connector P14, Pin c10 (TTL level)
RXDB	25	I	RX DATA Channel B, DATAPORT P2 (RS232 level)
TXDB	24	O	TX DATA Channel B, DATAPORT P2 (RS232 level)
OP0/RTSA-	29	O	RTS Channel A, P1, Pin 5 (RS232 level) & To IO Expansion Connector P14, Pin c12 (TTL level)
OP1/RTSB-	23	O	RTS Channel B, DATAPORT P2 (RS232 level)
OP4/RXRDYA-	27	O	SFX Channel #1 – U8, Pin S1 (Select Sample Rate)
OP6/TXRDYA-	26	O	SFX Channel #1 – U8, Pin S2 (Select Sample Rate)
CTSA-	28	I	CTS DUART Channel A, P1, Pin 4 (RS232 level) & To IO Expansion Connector P14, Pin c11 (TTL level)
CTSB-	22	I	CTS Channel B, DATAPORT P2 (RS232 level)

6.4.5 Timer Module

The Timer Module provides 2 General Purpose Timers.

The Pluto 5 Board uses these to provide a variable duty-cycle signals on TOUT1 and TOUT2 that is used to control the volume setting on each channel of the TDA7057AQ Stereo Audio Amplifier.

Timer 1 (TOUT1) controls the volume of Sound Channel #1. Timer 2 TOUT2) controls the volume of Sound Channel #2 if it is fitted. If Sound Channel #2 is not fitted, then Timer 2 may be used for other purposes.

See Section 7.9, “Making Sounds” for detailed information on the operation of the Volume Controls.

Pins TGATE1- and TGATE2- are allocated as general purpose inputs which are used to read the SCL and SDA lines on the External I^2C Connector, P13.

Pins controlled by the Timer Module are allocated as follows:

Table 4. Allocation of MC68340 Pins Controlled by Timer Module

PIN	NO.	I/O	FUNCTION
TGATE1-	79	I	Read External I^2C line SCL on P13, Pin 3 (inverted)
TIN1	81	I	Not Used – Strapped To Vcc
TOUT1	80	O	Variable Duty Cycle Volume Control SFX Channel #1
TGATE2-	36	I	Read External I^2C Line SDA on P13, Pin 2 (inverted)
TIN2	34	I	Not Used - Strapped To Vcc
TOUT2	35	O	Variable Duty Cycle Volume Control SFX Channel #2

6.5 FPGA

The Pluto 5 Casino Controller is fitted with an 84 lead PLCC socket, position U6, into which is plugged an FPGA. The standard FPGA type used is an Actel A40MX04-PL84. The purpose of fitting an FPGA to the system is twofold. First, to allow the Pluto 5 Casino Controller to be uniquely configured for each user of the system to give commercial and software security (see **FPGA SECURITY MANUAL**). Secondly, it allows particular advanced features, for example, the EPROM Autoselect and Multiplex dimming, to be economically implemented.

The following main functions are carried out by the FPGA:

- Control automatic EPROM mode selection
- Generate control signals for on-board EPROM and RAM
- Generate control signals for Memory Expansion Connector P15.
- Generate DMA requests and multiplex data for Sound Channels 1 & 2.
- Control and drive of data to Multiplex Arrays, both on-board MPX1 and expansion MPX2.
- Provide various levels of Software Security.
- Form an oscillator with 14.75MHz resonator:
- Generate Main Clock, EXTAL for MC68340 Processor @32.768kHz.
- Generate clock for MC68340 Serial Module @3.6864MHz.
- Generate clock for OKI MSM6585 devices, U8/39 @640KHz.

6.6 EPROM Sockets / EPROM Autoselect Feature

The 2 EPROM positions, U1 and U2, are configured such that 4 possible configurations of programme memory are possible (assuming no external memory expansion via P15):

Table 5. Possible EPROM Configurations

U1	U2	Mode	Configuration	Total Size	Addresses scrambled
27C040	omit	8 bit	512k*8	512Kbyte	no
27C040	27C040	16 bit	512K*16	1Mbyte	yes
27C801	omit	8 bit	1024k*8	1Mbyte	no
27C801	27C801	16 bit	1024k*16	2Mbyte	yes

It is not necessary to change any links on the board in order to switch between different memory configurations. All relevant switching is carried out within the FPGA, which contains an “EPROM Autoselect” feature. After Power-up, during the reset period, the FPGA reads the top byte address of U1. Data contained in this byte defines the memory configuration required and the FPGA sets up the control lines to the EPROM sockets accordingly, so that, at the end of reset, the processor is able to read the EPROM(s) correctly.

Thus, after the final linked EPROM software module has been created, prior to being blown into EPROM, the top location of the memory must be overwritten with suitable data to signify the EPROM configuration that will be used.

This is the feature referred to as **EPROM Autoselect**. A full operational description of this feature is given in the User manual for the FPGA in use on the Pluto 5 Casino Controller Board.

As with the Pluto 1 System, in order to facilitate the option to use either 1 or 2 EPROMs, i.e. run in 8 bit or 16 bit mode, it is necessary to have some scrambling of the address lines to the EPROMs when operating in 16 bit mode. Therefore, prior to blowing 16 bit EPROMs, the data must be re-arranged to compensate. A software utility is provided with the Pluto 5 Development Kit to carry this out.

Note that this scrambling of address lines is applicable **ONLY** to sockets U1 and U2 on the **Pluto 5 Casino Controller Board**. Any EPROM sockets on **Memory Expansion Cards** are connected 1:1 to the address bus and do **NOT** require any special processing.

6.7 EPROM Address Line Scrambling in 16 Bit Mode

*6.7.1 2*27C040 EPROMs*

In 16 bit mode, running with 2 * 27C040 EPROMs, the scrambling of the address lines cause the following effect on the memory mapping in the EPROMs. Note that this table applies to the re-mapping that occurs to the EPROM contents, rather than the actual address lines.

Table 6. Re-Mapping of Address Lines in 2*27C040 Mode

68340 Address Bus	EPROM Address
A0	Not Used in 16 Bit Mode
A1-A18	A2-A19
A19	A1

Thus, for example, addresses will be translated as follows so the contents of the EPROM must be re-arranged to compensate:

Table 7. Re-Mapping of EPROM Contents in 2*27C040 Mode

68340 Access Address	Will Read From This Location in EPROM
0000 0000	0000 0000
0000 0002	0000 0004
0000 0004	0000 0008
0000 0006	0000 000C
0000 0008	0000 0010
|	|
0007 FFFC	000F FFF8
0007 FFFE	000F FFFC
0008 0000	0000 0002
0008 0002	0000 0006
|	|
000F FFFC	000F FFFA
000F FFFE	000F FFFE

*6.7.2 2*27C801 EPROMs*

In 16 bit mode, running with 2 * 27C801 EPROMs, the scrambling of the address lines cause the following effect on the memory mapping in the EPROMs. Note that this table applies to the re-mapping that occurs to the EPROM contents, rather than the actual address lines.

Table 8. Re-Mapping of Address Lines in 2*27C801 Mode

68340 Address Bus	EPROM Address
A0	Not Used in 16 Bit Mode
A1-A18	A2-A19
A19	A1
A20	A20

Thus, for example, addresses will be translated as follows so the contents of the EPROM must be re-arranged to compensate:

Table 9. Re-Mapping of EPROM Contents in 2*27C801 Mode

68340 Access Address	Will Read From This Location in EPROM
0000 0000	0000 0000
0000 0002	0000 0004
0000 0004	0000 0008
|	|
0007 FFFC	000F FFF8
0007 FFFE	000F FFFC
0008 0000	0000 0002
0008 0002	0000 0006
|	|
000F FFFC	000F FFFA
000F FFFE	000F FFFA
0010 0000	0010 0000
0010 0002	0010 0004
0010 0004	0010 0008
|	|
0017 FFFC	001F FFF8
0017 FFFE	001F FFFC
0018 0000	0010 0002
0018 0002	0010 0006
|	|
001F FFFC	001F FFFA
001F FFFE	001F FFFA

6.8 Memory Expansion

Various optional memory cards may be fitted to the Memory Expansion Connector P15. Seven lines from the FPGA are included along with 16 data lines and 21 address lines.

The default functionality of the FPGA lines allows memory cards fitted with up to 4 EPROM or FLASH devices to be accommodated along with a pair of RAM devices with no additional mapping components.

If a memory card is fitted with 5V FLASH devices, then Write facilities are available. EPROM Autoselect is also available with devices fitted on a Memory Card.

6.9 Open Drain Outputs, OP0-63

A block of 64 Open Drain Outputs, OP0-63, are provided by 8 off TPIC6259 devices U22-U29 (see Figure 6 - Schematic Sheet 6 – Open Drain Outputs)

These are memory mapped as the least significant byte of a block of 8 words of address space. The chip select for these devices, CS_OP-, is provided by the FPGA. Consult the User Manual of the FPGA being used for exact mapping.

Please note that the chips are bit wide, not byte wide. Thus, Bit 0 of each word drives one device, U22: Bit 1 drives U23, etc.

Table 10. Mapping of Open Drain Outputs (OP0-63) to TPIC6259 Devices

Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Pin	**U29**	**U28**	**U27**	**U26**	**U25**	**U24**	**U23**	**U22**	*Addr.*
Q7	OP63	OP62	OP61	OP60	OP59	OP58	OP57	OP56	Base+14
Q6	OP55	OP54	OP53	OP52	OP51	OP50	OP49	OP48	Base+12
Q5	OP47	OP46	OP45	OP44	OP43	OP42	OP41	OP40	Base+10
Q4	OP39	OP38	OP37	OP36	OP35	OP34	OP33	OP32	Base+8
Q3	OP31	OP30	OP29	OP28	OP27	OP26	OP25	OP24	Base+6
Q2	OP23	OP22	OP21	OP20	OP19	OP18	OP17	OP16	Base+4
Q1	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8	Base+2
Q0	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Base+0

Basically, the drive capability of these devices is 250mA per output, continuous, with all outputs ON. If less than 8 outputs are ON in any one package, or any outputs are operating with a small load, the capacity of the other outputs increases. For example, at 25°C, the TPIC6259 can sink 400mA continuously from 3 outputs. Please refer to the data sheet for the TPIC6259 (tpic6259.pdf) for details.

When allocating any output to a load greater than 250mA, consideration should be given to the loading on each device. See Section 5.1, “Driving Reels” for details on driving standard reel mechanism stepper motors.

Note also that, because they are MOSFETs, the outputs are resistive (<2Ω) and do not suffer from the minimum saturation voltage of about 1V which would be the case if they were darlingtons. Therefore, at low currents, they pull down close to Gnd and may be safely used to drive TTL Inputs, Switch Strobes, Coin Mechanism Enables, etc.

6.10 AUX Outputs, AUX0-7

8 auxiliary TTL level open drain outputs are provided by U30 (see Figure 9 - Schematic Sheet 9 – IO Connectors). U30 is a TPIC6B259 which functions exactly the same as the TPIC6259 devices used to drive OP0-63, but with a lower drive capability (see data sheet “tpic6b259.pdf”).

On the Standard Pluto 5, they are memory mapped as the least significant bit of a block of 8 bytes of address space at an address determined by the FPGA fitted to the board.

However, on the Pluto 5 Casino Controller, they are selected by the same line as the 64 Open drain outputs, OP0-63, via 1/2 74HCT139, U52.

They are open drain outputs fitted with 1K pull-up resistors to Vcc.

AUX0-5 are routed to connector P12 “AUX OUTPUTS”.

AUX6-7 are routed to Connector P13 “I^2C”.

6.11 Inputs, IP0-31

External inputs are catered for by 32 input lines, IP0-31, shown on Schematic Sheet 7. Like the Open Drain outputs these are memory mapped as the least significant byte of a block of 4 words of address space.

Each input is provided with a 3K3 pull-up resistor to Vcc (+5V) and feeds into a 74HC family device (rather than 74HCT). This give the inputs a low level threshold of <1.5V and a high threshold of >3.5V. The 47K resistor in series with the input protects the 74HC253 devices from noise spikes or high voltages on the inputs.

The 1.5V low threshold allows the inputs to be safely driven as a multiplexed array with a diode in series with each switch with the strobes generated using a number of the Open Drain Outputs, OP0-63, described above.

The 32 inputs are mapped as shown in the following table. The top 4 bits of each word are read as “1”s and bits 8 to 11 contain the DIL Switch Settings (as described in the next section). The base address is defined by the FPGA.

Table 11. Mapping of Inputs IP0-31

	D15-12	D11-8	D7	D6	D5	D4	D3	D2	D1	D0
Base+6	0xF	DIL SW	IP31	IP30	IP29	IP28	IP27	IP26	IP25	IP24
Base+4	0xF		IP23	IP22	IP21	IP20	IP19	IP18	IP17	IP16
Base+2	0xF		IP15	IP14	IP13	IP12	IP11	IP10	1P9	IP8
Base	0xF		IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0

6.12 DIL Switches

The Pluto 5 board is equipped with two 8 way DIL Switches, SW1 and SW2. These are read at the same addresses as the 32 Inputs (see preceding Section).

Table 12. Mapping of DIL Switch Inputs

	D15-D12	D11	D10	D9	D8	D7-D0
Base+6	0xF	SW2:8	SW2:7	SW1:8	SW1:7	IP31-24
Base+4	0xF	SW2:6	SW2:5	SW1:6	SW1:5	IP23-16
Base+2	0xF	SW2:4	SW2:3	SW1:4	SW1:3	IP15-8
Base	0xF	SW2:2	SW2:1	SW1:2	SW1:1	IP7-0

6.13 Software Controlled Indicator LED

LD2 is a green LED that may be turned on or off under software control (see Schematic Sheet 9). The LED may be used to provide an indication that software is running or perhaps for fault diagnosis.

The PORTA2 line from the MC68340 SIM40 Module drives the LED. After reset, the PORTA pins are high impedance and pulled high by resistor network N11. This signal passes through the inverter U7F which thus turns ON the LED. Therefore, initially and with no action on the part of the software, the LED will be ON indicating that Vcc is present.

If the software sets PORTA2 pin as an output and drives it low, the LED will go OFF.

The PORTA pins are taken to the I/O Expansion Connector P14. Future I/O Expansion Cards may use the PORTA2 pin for some other function, in which case this will have to be taken into consideration when operating the indicator LED.

6.14 On-board Push Button

A Push Button Switch, SW3, is provided on the board (see Schematic Sheet 2). The function of this switch is at the discretion of the user of the board.

It is connected so as to pull the PORTA3 line from the MC68340 SIM40 Module to GND when operated.

The PORTA pins are taken to the I/O Expansion Connector P14. Future I/O Expansion Cards may use the PORTA3 pin for some other function, in which case the possible interaction with SW3 will have to be taken into account.

6.15 Multiplexer

The **Pluto 5 Casino Controller** provides hardware assistance (within the FPGA) to the Processor allowing a single 32*16 Multiplex Array (MPX1) to be controlled.

The **Pluto 5 Casino Controller** has ½ of MPX1 configured as a 16*16 (256) Lamp Drive Array and the other ½ configured as a 16*16 (32 seven-segment digits) LED Drive Array.

The Lamp Multiplex Drive Circuitry is designed to drive 12V, 100mA bulbs. However, it is permissible for a small number (up to 16) of positions to drive either a higher power bulb (12V, 180ma) or a pair of 100mA bulbs. These "high load" positions should be arranged such that no more than one is on any one Row or Column drive.

The Lamp Multiplexer will normally be driven from a 48V dc supply (Vmpx) and run with a 1 in 16 duty cycle which allows the maximum complement of 256 lamps to be driven. However, if necessary, a 36V

supply may be used provided the duty cycle is reduced to 1 in 8, which has the side effect of reducing the drive capability to 128 lamps and 128 LEDs (16 seven-segment digits).

The Multiplex Array has hardware assistance from the FPGA to enable dimming control. Dimming level may be set independently for each of the 16 Column strobes, e.g. the 8 lamps on one Column Strobe could be set to one brightness level while the 8 lamps on a different Column Strobe could be set to another brightness. The overall basic timing of the multiplexing remains under software control allowing “overdrive” of lamps for special effects.

Dimming is achieved changing the data presented to the Lamp Row / LED Segment drives at an adjustable time within the 1mS strobe time. Thus each lamp/LED has two bits of data associated with it in software – the first bit is the data applied during the first part of the 1mS Strobe period, the second bit is applied during the second period. The duration of the period that the first bit is applied for may be set in units of 1/16 mS.

The multiplex is software driven. Every 1mS, data for the next strobe is written to the FPGA which in turn formats and serialises the data before clocking out the MPX1 data to the on-board 4094 shift registers (U18,U19,U20,U21,U35,U36).

The exact format of the data to be written each millisecond is determined by the design of the FPGA being used, but in general it is as follows.

- 32 bits of MPX1 Row/Segment data. First period data.
- 32 bits of MPX1 Row/Segment data. Second period data.
- 4 bits defining Column/Digit strobe number to activate.
- 4 bits defining First Period duration (units of 62.5µS).

Consult the User Manual of the actual FPGA in use for exact details of operation.

6.16 Multiplexed Lamp Current Sense

A facility is provided to allow the processor to check the 256/128 possible lamp positions of MPX1 to determine:

a. Is a light bulb present?
b. Is there a short circuit in this position?

This facility is intended to be run at power up and, perhaps, as a production test. The facility cannot be used during normal operation of the machine.

A resistance of approximately 24mΩ is implemented, as a copper track on the PCB, between common source connection of all the Lamp Column/LED Digit sinks, Q35-50 and Gnd (see Schematic Sheet 11). The voltage across this resistor is compared against 2 thresholds formed by resistor chain R124, R125 and R126 by comparators U16C and U16D (see Schematic Sheet 8). These thresholds correspond to nominal currents of about 375mA and 4.8A.

The outputs of the 2 comparators, U16C and U16D are connected to processor lines PORTA6 and PORTA7. The current sensing comparators may be disabled by SFX_CLK being enabled. When SFX_CLK, a 640kHz clock, is enabled by setting a bit in the FPGA (see **FPGA USER MANUAL**), the “+” inputs of the 2 comparators are pulled up to about +5V by D21/C9/C10 which forces the comparator outputs (which are open collector) OFF. In this state the lines PORTA6 and PORTA7 are free to be used as outputs driving the S1 & S2 pins of SFX Channel #2 or as required by any card fitted to the I/O Expansion Connector, P14. When the SFX-CLK is turned OFF (and forced low), any voltage on C9/10 is discharged by R127, and the current sensing circuit is enabled.

With no current through the Column/Digit Sinks, both outputs PORTA6/7 will be LOW because V+ < V- on the comparators. When the current through the 24mΩ resistor exceeds a nominal 375mA, PORTA6 will go high. When the current exceeds a nominal 4.8A, PORTA7 will also go high.

The sequence of operation to test a lamp is as follows:

- Turn off SFX_CLK in FPGA to enable circuit.
- Turn off all Row/Digit drives on MPX1.
- Ensure PORTA6 and PORTA7 both read 0
- Turn on lamp to be tested on multiplex by writing appropriate data to FPGA.
- Start a 1mS timer.
- Loop watching lines PORTA6 and PORTA7.
- If PORTA7 line goes high, there is a short circuit in this position, so immediately disable the multiplex drives by turning off Multiplex OE line in the FPGA.
- If PORTA6 line goes high but not PORTA7, then there is a light bulb connected and apparently working.
- If 1mS timer times out without either line going high, then either no bulb present or it is open circuit.
- Record result and go on to next bulb.
- When complete, act as required on results. Re-enable SFX-CLK to allow Sound Channels to work.

6.17 Sound Generation

The sound generation circuits are shown on Schematic Sheet 5, Figure 5.

U8 and (optionally) U39 are the source of Sound Channel 1 & 2 respectively with the audio output being pin 10, Aout. These OKI MSM6585 devices are 4 bit ADPCM D-A converters capable of running at sample rates of 4KHz, 8KHz, 16KHz or 32KHz. This rate is selected by software by setting levels on the S1 and S2 pins. On Channel 1 (U8) these pins are controlled by the OP4 and OP6 lines from the MC68340 Serial Module. On Channel 2 (U39) these pins are controlled by the PORTA6 and PORTA7 lines from the MC68340 SIM40 Module.

The VCK- output from the MSM6585 is a square wave at the sampling frequency selected by S1 and S2. The MSM6585 reads the 4 bit sample immediately after the rising edge of VCK-.

The VCK- from the MSM6585 is connected to the FPGA where it is divided by 2 to produce a DMA Request signal to the processor. Sound data is transferred, a byte at a time (1 byte = 2 * 4 bit sound samples), to the appropriate register within the FPGA by the DMA Module if a sound is being played. The FPGA in turn presents alternately the high and low nibble to the MSM6585 OKI chip.

The sound channel requests a byte of data (via the FPGA) at half the sound sample rate. E.g., if the MSM6585 has been set to run at 16KHz sample rate, the FPGA will issue DMA requests at 8KHz.

These requests are issued continuously to the DMA Module, but in times of silence, the DMA channels are inactive and therefore no new data is transferred into the FPGA sound register. In this case, the user must ensure that the last data written to the FPGA sound register before a period of silence is 0x80. This will ensure that, during a silent period, the MSM6585 is being continuously fed a repeated sequence of alternate 0x8 and 0x0 nibbles. This keeps the ADPCM converter in its quiescent state. If the sound data is generated using the Heber Sound Solutions software, the last byte of the data is always 0x80, so this condition will automatically be satisfied.

Sound Channel 1 (U8) is fitted as standard and uses DMA Channel 1. Sound Channel 2 (U39) is optional and uses DMA Channel 2.

The RESET pin of each channel is under individual software control. Pin PORTA0 drives SFX Channel #1 RESET. Pin PORTA1 drives SFX Channel #2 RESET. After Power –Up, these pins will default to being inputs and therefore the Resistor network N11 will pull them High, holding both Sound Channels in a RESET state. Before the Sound Channels can be used, these two pins must be set as outputs by the SIM40.

6.18 Stereo Amplifier and Volume Controls

The Stereo Amplifier is shown on Schematic Sheet 5, Figure 5.

U32 is a Philips TDA7057AQ Stereo Audio Amplifier with independent DC volume controls. Note that the loudspeaker outputs, on Connector P10, are bridge driven so neither of the loudspeaker wires may be connected to Gnd.

The DC volume controls of the TDA7057 work over the range 0.4V(min) to 1.2V (Max). The variable duty cycle outputs on pins TOUT1/2 from the two timers in the MC68340 Timer Module are integrated by the combination of two 3K3 resistors and a 1µF capacitor (R108, R109, C45 on Channel 1: R110, R113, C46 on Channel 2) to provide the control voltage needed. The control voltage is given by the formula 2.5*{duty cycle} where "duty cycle" is the proportion of the time that the TOUT Pin is HIGH.

Normally, Sound Channel 1 (U8, DMA Channel 1) feeds Amplifier Section 1 (volume control - Timer Channel 1) driving LS1. Sound Channel 2 (U39, DMA Channel 2) feeds Amplifier Section 2 (volume control – Timer Channel 2) driving LS2.

A pin on the Loudspeaker Connector, P10, pin 3, which allows the output signal from Amplifier Channel 1 to be fed back into the input of Amplifier Channel 2. This allows various alternative modes of operation, for example, if only Sound Channel 1 is fitted, then by linking the LS1+ output to the feedback pin, the same signal can drive BOTH loudspeakers. See Section 7.9, "Making Sounds" below for a more detailed explanation of the different operational modes that are possible.

6.19 Serial I/O

P1 provides connections to RS232 Channel A, Data Receive & Transmit plus RTS/CTS.

P2 provides connections to RS232 Channel B, Data Receive & Transmit plus RTS/CTS and is in the format specified by the BACTA standard.

Operation of the above two ports is determined by the operation of the Serial Module in the MC68340 Processor. Refer to the Serial Module Section of **Motorola MC68340 User Manual** for a full explanation.

6.20 Internal I^{2}C Bus

An internal I^{2}C Bus is implemented using SIM40 Lines PORTA4 (SCL) and PORTA5 (SDA). This bus allows the processor to read and write the optional Real Time Clock chip, U40, and the optional E^{2}PROM, U37. If neither of these devices is fitted, then these 2 lines are also available on the I/O Expansion Connector P14 and are free for other uses.

6.20.1 Real Time Clock

U40 is a position that accepts a Philips PCF8583 I^{2}C Real Time Clock. The standard Pluto 5 Casino Controller has a socket fitted in this position along with the 32.768KHz Crystal, X2. However, the PCF8583 IC is NOT fitted as standard but is available as an optional extra or may be fitted by the user.

The I^{2}C Slave Address of the RTC is as follows:

Table 13. I^{2}C Slave Addresses for RTC, U40

READ:	0xA1
WRITE:	0xA0

6.20.2 E^{2}PROM

U37 position is fitted with a socket that accepts an "Industry Standard" E^{2}PROM, 24C04 (512 bytes) or 24C08 (1024 bytes) with pin 7, which serves a different function on devices from different manufacturers, connected to GND. The Pluto 5 Casino Controller Boards, as standard, do not have an E^{2}PROM fitted but they are available as an optional extra or may be fitted by the user.

We strongly recommend that, if a user supplies or fits his own devices, that only NM24C04 or NM24C08 devices should be used (manufactured by Fairchild or National Semiconductor). Heber cannot offer Technical Support for the use of devices from alternate manufacturers.

To avoid a clash of I^2C addressing between the PCF8583 RTC and the 24Cnn E^2PROM, A2 (Pin 3) of the E^2PROM is strapped to Vcc and A0/A1 to GND and this socket is restricted to accepting devices no larger than the 24C08. Note, however, that there is no such size restriction on the devices that may be connected via P13, the External I^2C Bus Connector.

The I^2C Slave Address of each of the 256 byte “Page Blocks” in the E^2PROM, U37, is as follows:

Table 14. I^2C Slave Addresses for E^2PROM, U37

	BLOCK 0 *24C04 or 24C08*	**BLOCK 1** *24C04 or 24C08*	**BLOCK 2** *24C08 only*	**BLOCK 3** *24C08 only*
READ	0xA9	0xAB	0xAD	0xAF
WRITE	0xA8	0xAA	0xAC	0xAE

6.21 Serial Channels C-H

Three 44 lead PLCC sockets are provided, U53, U54 and U55, into which may be fitted 68681 or 68692 DUARTs.

These are mapped as 8 bit devices by the FPGA. Please consult the User Manual for the FPGA being used for details of mapping.

- Channel C is buffered to RS232 levels and taken to 9 way D Type Plug, P17, to provide a PC-AT compatible Serial Port with lines RX, TX, RTS, CTS, DST, DTR & CD. Control line RI is not implemented.

- Channels D-G are buffered to RS232 levels and taken to connector P18. Only RX, TX, RTS & CTS lines are provided on these channels.

- Channel H is buffered to TTL levels by non-inverting buffer U49 and taken to P19. 3 Input and 3 Output control lines are provided in addition to the RX and TX data lines.

6.21.1 Mapping of DUART Lines

The I/O lines of the DUARTs are mapped as shown in the following tables:

U53 – Channels C & D			
Pin	**Channel**	**Name**	**Comments**
TXDA	C	TXDC	RS232 Level to P17-3
RXDA	C	RXDC	RS232 Level to P17-2
TXDB	D	TXDD	RS232 Level to P18-7
RXDB	D	RXDD	RS232 Level to P18-5
OP0	C	RTSC	RS232 Level to P17-7
OP1	D	RTSD	RS232 Level to P18-6
OP2	-		No connection
OP3	-		No connection
OP4	-		No connection
OP5	-		No connection
OP6	-		No connection
OP7	-		No connection
IP0	C	CTSC	RS232 Level to P17-8
IP1	D	CTSD	RS232 Level to P18-8
IP2	C	DSRC	RS232 Level to P17-6
IP3	C	CDC	RS232 Level to P17-1
IP4	-	-	Strapped to VCC
IP5	-	-	Strapped to VCC

Table 15 - Mapping of DUART U53 I/O Pins

U54 – Channels E & F			
Pin	**Channel**	**Name**	**Comments**
TXDA	E	TXDE	RS232 Level to P18-13
RXDA	E	RXDE	RS232 Level to P18-11
TXDB	F	TXDF	RS232 Level to P18-19
RXDB	F	RXDF	RS232 Level to P18-17
OP0	E	RTSE	RS232 Level to P18-12
OP1	F	RTSF	RS232 Level to P18-18
OP2	-	-	No connection
OP3	-	-	No connection
OP4	-	-	No connection
OP5	-	-	No connection
OP6	-	-	No connection
OP7	-	-	No connection
IP0	E	CTSE	RS232 Level to P18-14
IP1	F	CTSF	RS232 Level to P18-20
IP2	-	-	Strapped to VCC
IP3	-	-	Strapped to VCC
IP4	-	-	Strapped to VCC
IP5	-	-	Strapped to VCC

Table 16 - Mapping of DUART U54 I/O Pins

U55 – Channels G & H			
Pin	**Channel**	**Name**	**Comments**
TXDA	G	TXDG	RS232 Level to P18-25
RXDA	G	RXDG	RS232 Level to P18-23
TXDB	H	TXDH	TTL Level to P19-3
RXDB	H	RXDH	TTL Level to P19-5
OP0	G	RTSG	RS232 Level to P18-24
OP1	H	RTSH	TTL Level to P19-7
OP2	H	OP2	TTL Level to P19-11
OP3	H	OP3	TTL Level to P19-13
OP4	-	-	No connection
OP5	-	-	No connection
OP6	-	-	No connection
OP7	-	-	No connection
IP0	G	CTSG	RS232 Level to P18-26
IP1	H	CTSH	TTL Level to P19-9
IP2	H	IP2	TTL Level to P19-15
IP3	H	IP3	TTL Level to P19-17
IP4	-	-	Strapped to VCC
IP5	-	-	Strapped to VCC

Table 17 - Mapping of DUART U55 I/O Pins

6.21.2 DUART Interrupts

The interrupt outputs from the 3 DUARTs are connected in parallel (wire-ored) and taken to IRQ5-/PB5 pin on the 68340 processor.

Note that IRQ5- must be run in Autovector mode and software must poll the 3 DUARTs to establish the source of the interrupt.

Note also that if a Video Card is added on P14 & P15, that IRQ5- may also be used as a Video Interrupt and the software must poll accordingly.

6.22 Secondary RAM

U50 is a 32Kx8 RAM, completely independent of the main RAMs, U3 and U4. It is battery backed, either by the Primary Backup Battery (see Section 6.3 above) if JP5 is fitted or by the Secondary Backup Battery BT2 (if fitted).

The RAM is mapped as a Byte Wide Port at an address determined by the FPGA.

6.23 Security PIC Microcontroller

U51 is a socket for an optional PIC16C54 microcontroller.

It is powered by a battery backed supply and therefore continues to run when the controller is powered down. The oscillator crystal is 32.768KHz to reduce power consumption.

Details of operation will be found in the Heber User Manual of the device fitted.

7 MACHINE OPERATION

This section discusses how various standard amusement machine functions can be implemented.

7.1 Driving Reels

Up to six 12V Stepper Motor Reel Mechanisms may be connected to the “REEL” connector, P7. +12V outputs are available for the motor common connection and GND/Vcc are available for the Opto supply. A 6*6 subset of the Lamp Multiplex is configured so up to 6 lamps per reel may be accommodated, in either “sinking” or “sourcing” mode (depending on the wiring of the Reel Mechanism. 6 inputs, IP0-5, are provided for the Opto Inputs

When driving stepper motor reels, because the maximum (static) current load of each winding is 400mA (assuming 30Ω,12V windings), it is important to connect the motors to distribute the load evenly amongst the TPIC6259 driver chips.

The recommended method of connection is to wire the reel motors as follows:

Table 18. Recommended Reel Stepper Motor Drive Connections

REEL 1	OP0-3
REEL 2	OP4-7
REEL 3	OP8-11
REEL 4	OP12-15
REEL 5	OP16-19
REEL 6	OP20-23

This guarantees that a maximum of 3 motor windings are driven simultaneously by any one TPIC6259 device which is within the ratings of the device even under the worst case of a reel being stationary and unchopped. Of course, when the motor is running or is being chopped the average current drops significantly.

Extra reels could be connected via pins on the other connectors. Providing the software chops the current to the reels when they are not spinning, an extra 2 reels can be wired to OP24-27 and OP28-31 and should allow the TPIC6259s to remain within their ratings.

NB: The +12V outputs on P7 Pins 45-50 are fed directly from the +12V Input to the Pluto 5 Board on P3, Pin 4. It does not go via Fuse F1 on the board.

7.2 Reading the DIL Switches

The state of the DIL Switches may be read at any time by reading the memory locations as described in Section 6.12 above.

7.3 Reading the Switch Inputs

The 32 switch inputs may be read at any time by reading the memory locations as described in Section 6.11 above.

In most applications, these inputs should be debounced in software. A typical debounce algorithm might be to read the switches every 1mS, but only register a change of state on the input after it has been stable for 3 consecutive readings.

It is possible to implement, say, a 64 multiplexed switch input array by using, 8 of the Open Drain Outputs OP0-63 as strobes and 8 of the Inputs IP0-31. In this case, a diode would need to be connected in series with each switch.

7.4 Interfacing to Coin & Note Acceptors

Most Coin or Note Acceptors have open collector ("sink to ground") outputs. These may be connected directly to any of the Pluto 5 Inputs (IP0-31). Mechanism "Enable" or "Control" inputs may usually be driven directly from any of the Pluto 5 Open Drain Output lines (OP0-63).

7.5 Interfacing to Coin Payout Mechanisms

Payout Hoppers that require relatively low drive currents, e.g. Coin Controls Universal Hopper, may be driven directly from an Open Drain Output. Higher current devices, such as 50Vac or 24Vdc Payout Solenoids, should be driven using Open Drain Outputs via a suitable Triac or Relay Interface Card. Heber produces a number of suitable interfaces.

7.6 Driving Vacuum Fluorescent Displays (VFD)

The standard VFD/Linewriter display used in most Gaming/Amusement Machines is driven by 3 TTL level signals, Clock, Data and Reset.

Connector P12 has 6 TTL level outputs which could drive up to 2 display modules.

The mapping of these outputs as the LSB of 6 bytes makes it convenient for the software to implement the bitwise drive required.

7.7 Using the External I^2C Bus

Connector P13 is intended for driving external boards containing I^2C Bus components. A common use for this could be the provision of a removable E^2PROM Module for use in Spain or any other country with a similar requirement.

Heber have available a small PCB containing a NM24C04 or NM24C08 E^2PROM that plugs directly on to P13.

On this connector, the SDA line is driven by the Open Drain Output, AUX7 and may be read by the 68340 Timer Module as the (inverted) TGATE2- signal.

Similarly, the SCL line is driven by AUX6 and read by TGATE1.

Note, On the Pluto 5 Casino Controller, these 2 lines are also connected to the internal Security PIC Microcontroller which acts as an I^2C slave device. Care must be taken to avoid possible conflicts between the PIC and any external I^2C device connected on this bus.

7.8 Driving Meters

Electromechanical Meters or Counters should be 12V DC parts. The common +12V supply to them should be the Vmeter+ supply from Connector P9 ("I/O 2"), pin B17 and each should be driven by an Open Drain Output (OP0-63).

As the meter is pulsed ON, the software should check that the Vmeter Current Sense Input has operated, i.e. that pin PORTB4 has gone high.

Because of possible delays in responding to a meter being turned on it is recommended that the software checks the current sense pin immediately before the meter is turned OFF at the end of a pulse. To detect tampering or a failure of the current sense circuitry, the software should also check that the current sense pin goes LOW when no meter is operated.

7.9 Making Sounds

Loudspeaker outputs on connector P10 are bridge driven, so do **NOT** connect either connection of a loudspeaker to ground or to any other loudspeaker drive. Ideally 8Ω loudspeaker(s) should be used, but higher impedance components could be used without any risk of damage to the amplifier. The use of 3 or 4ohm loudspeakers should be avoided.

It is possible to run the sound in a number of different modes:

7.9.1 Single Channel/Single Speaker (Mono) Mode

This is the lowest cost option, using the standard Pluto 5 Board with a single loudspeaker.

The optional SFX Channel 2, U39, is not fitted and only SFX Channel 1, U8, is operational. A single loudspeaker is connected to LS1 pins (1 & 2) only. Pins 3,4,5 should be left open.

7.9.2 Single Channel/Dual Speaker Mode

This mode still uses the standard Pluto 5 Board with only SFX Channel 1, U8, operational, but allows the use of 2 loudspeakers to improve the quality or quantity of the sound.

One loudspeaker, LS1, is connected between Pins 1 & 2 of P10. The second loudspeaker, LS2, is connected between Pins 4 & 5 of P10. A wire should also be fitted joining together Pins 1 & 3 of P10, which allows the sound from SFX Channel 1 to be reproduced via Amplifier Channel 2.

The Channel 1 Volume Control will control the overall volume heard from both speakers, while Channel 2 Volume Control may be used to control “Balance”, allowing an adjustment of the level of sound heard from LS2 relative to LS1. If Channel 2 Volume is fixed at 7 or 8 (where 15 is maximum), this will result in approximately equal sounds being heard from each speaker and the overall volume may be controlled by the Channel 1 Volume Control.

7.9.3 Dual Channel/Dual Speaker (Stereo) Mode

In Stereo Mode, the optional second channel IC U39 is fitted and 2 loudspeakers are used, connected to LS1 and LS2 pins. Pin 3 is left open. Channel 1 Volume Control will adjust the level of LS1, Channel 2 Volume Control will adjust the level of LS2.

In this mode true stereo sound effects may be reproduced, although the subjective effect heard by the player will depend upon the placement of the loudspeakers in the cabinet.

7.9.4 Dual Channel/Single Speaker Mode

This mode may be used when the Pluto 5 Casino Controller is used in a cabinet containing only 1 loudspeaker, but has the optional Channel 2 IC, U39, fitted.

The single loudspeaker is connected to the LS2 pins, 4 & 5, of P10. A link is fitted between pins 1 and 3. This will allow sounds generated on Channel 1 to be heard through LS2 along with the sounds from Channel 2. Note that the Channel 2 Volume Control will adjust the overall volume of the sound heard from LS2 while the Channel 1 Volume Control will adjust the volume of Channel 1 relative to Channel 2.

If the Channel 1 Volume Control is fixed at 7 or 8, (where 15 is maximum), then sounds reproduced through either Channel 1 or Channel 2 will come out at approximately the same level and the overall volume may be controlled by the Channel 2 Volume Control.

7.10 Using Multiplexed Lamps

On all Multiplex lamp outputs, the Column Drives, LC0-15, SINK current to ground and the Row Drives, LR0-15, SOURCE current from the Lamp Supply (+36V or +48V). Thus, any lamps should be connected between a Row and a Column drive with their series diodes orientated with the cathode towards the Column Drive.

The choice of operation at 36V or 48V is determined by the Power Supply and the software. When running at 48V, the software will sequentially drive all 16 Columns, LC0-15, on a 1/16 duty cycle, each column being ON for 1mS and OFF for 15.

When running at 36V, the software will sequentially drive only the first 8 Columns (LC0-7) on a 1/8 duty cycle, each column being ON for 1mS and OFF for 7.

Please note that the multiplex circuitry is designed to drive 12V/100mA bulbs only.

7.11 Using Multiplexed LEDs

The multiplexed LED drive circuit is intended to be used with Common Cathode digits, either 7 segment plus decimal point or 14 segment. The common cathode connection of each digit should be connected to a digit drive output, DIG0-15, on connector P5. Each digit drive output can drive two 7 Segment Digits, the segment anodes for one connecting to drive SEG0-7 and the other to SEG8-15. By convention, segment “a” would connect to SEG0 or SEG8.

Alternatively, 14 segment starburst digits can be used, in which case each digit output would drive one digit and the 14 segment anodes should each be connected to one of the segment drive lines, SEG0-13.

The LED Digit drive circuitry shares the same Current Sink transistors as the Lamp Column drives. Thus, if the system is being driven in a 1/8 duty cycle to allow a 36V Lamp Supply, only Digit drive lines DIG0-7 are active. In this case only 16 Seven Segment LED digits may be driven from the controller.

7.12 Using the Multiplex Expansion Connector

The outputs on P11 are all CMOS signals swinging between GND and +12V. These signals may be connected to Pluto 5 Multiplex Expansion Boards to increase the Lamp and/or LED drive capability of the system.

See the **PLUTO 5 MULTIPLEX EXPANSION BOARD USER MANUAL** for details of connection and operation.

7.13 Adding Video Capabilities

A Calypso 16 Video Card is available from Heber Ltd. which plugs directly onto the Pluto 5 Casino board via the 2 DIN41612 connectors P14 and P15.

See the **CALYPSO 16 USER MANUAL** for details.

The Calypso 16 Video Card supersedes the Pluto 5 CGA/VGA Video Card. For further information on the Pluto 5 CGA/VGA Video Card refer to the **PLUTO 5 CGA/VGA BOARD USER MANUAL**.

8 SOFTWARE DEVELOPMENT

A number of options exist for the development and debug of software for use on Pluto 5.

Software will normally be generated using a Cross-Assembler, Cross Compiler and Linker package. A suitable package is included with the Pluto 5 Development Kit.

When software has been successfully compiled, assembled and linked, it may be tested and debugged using the Background Debug Mode facility built in to the 68340 Processor.

For full details of debugging, refer to the **PLUTO 5 DEVELOPMENT KIT QUICK START GUIDE** and other documentation supplied with the Development Kit.

9 CONNECTOR TYPES AND PIN OUTS

9.1 Schedule of Connector Types

There are two types of Pluto 5 Casino Board with either Ultrex or Box Header connectors, and 3 other families of connectors:

- Pluto 5 Casino with Ultrex connectors is referred to as **Pluto 5CU**
- Pluto 5 Casino with Box Header connectors is referred to as **Pluto 5CB**

Pluto 5CU uses the following 4 different families of connectors for connection to the cableform in the machine:

- AMPMTA-100. 2.54mm single in-line headers with friction lock and polarisation.
- AMP MTA-156. 3.96mm single in-line headers with friction lock and polarisation.
- AMP Ultrex. 2.54mm dual row headers.
- 25 way “D” Type

Pluto 5CB uses the following 4 different families of connectors for connection to the cableform in the machine:

- AMPMTA-100. 2.54mm single in-line headers with friction lock and polarisation.
- AMP MTA-156. 3.96mm single in-line headers with friction lock and polarisation.
- Tyco Box Header 2.54mm dual row headers
- 25 way “D” Type

The actual part numbers of the board headers fitted to the Pluto 5 Casino PCB along with the part numbers of suitable mating (cableform) parts are given in the following tables:

Table 19. AMP Ultrex Connector Part Numbers

Ident	Description	PCB Header AMP Part No.	AMP IDC Connector Part Number
			28-24 AWG Wire
P5	32W Ultrex	3-172870-2	3-172866-2
P7	50W Ultrex	5-172870-0	5-172866-0
P8	40W Ultrex	4-172870-0	4-172866-0
P9	34W Ultrex	3-172870-4	3-172866-4

Table 20. Tyco Box Header Connector Part Numbers

Ident	Description	PCB Header Tyco Part No.	Tyco IDC Connector Part Number
			28-24 AWG Wire
P5	34W Box Header	7-1437061-5	102387-8
P7	50W Box Header	9-1437061-5	102387-0
P8	40W Box Header	8-1437061-5	102387-9
P9	34W Box Header	7-1437061-5	102387-8

Table 21. AMP MTA-100 Connector Part Numbers

Ident	Description	PCB Header AMP Part No.	AMP IDC Connector Part Number	
			24 AWG (0.22mm^2) (Colour Natural)	22 AWG Wire(0.35mm^2) (Colour Red)
P1	6W MTA-100	640456-6	640621-6	640620-6
P4	18W MTA-100	1-640456-8	1-640621-8	1-640620-8
P6	16W MTA-100	1-640456-6	1-640621-6	1-640620-6
P10	5W MTA-100	640456-5	640621-5	640620-5
P11	7W MTA-100	640456-7	640621-7	640620-7
P12	8W MTA-100	640456-8	640621-8	640620-8
P13	4W MTA-100	640456-4	640621-4	640620-4

Table 22. AMP MTA-156 Connector Part Numbers

Ident	Description	PCB Header AMP Part No.	AMP IDC Connector Part Number	
			24 AWG (0.22mm^2) (Colour Natural)	20 AWG Wire(0.5mm^2) (Colour Yellow)
P3	6W MTA-156	640388-6	640429-6	640427-6

The above MTA-100 and MTA-156 IDC Connector Part Numbers are for illustration and are of the “Feed-Through Receptacle without Polarising Tabs” type. A number of alternatives exist that could also be used, for example “Closed-End” types. Please consult the relevant AMP information for an exhaustive list. If you have Internet Access, the information is also available on the AMP Web Site at http://www.amp.com/.

Strain relief covers are also available.

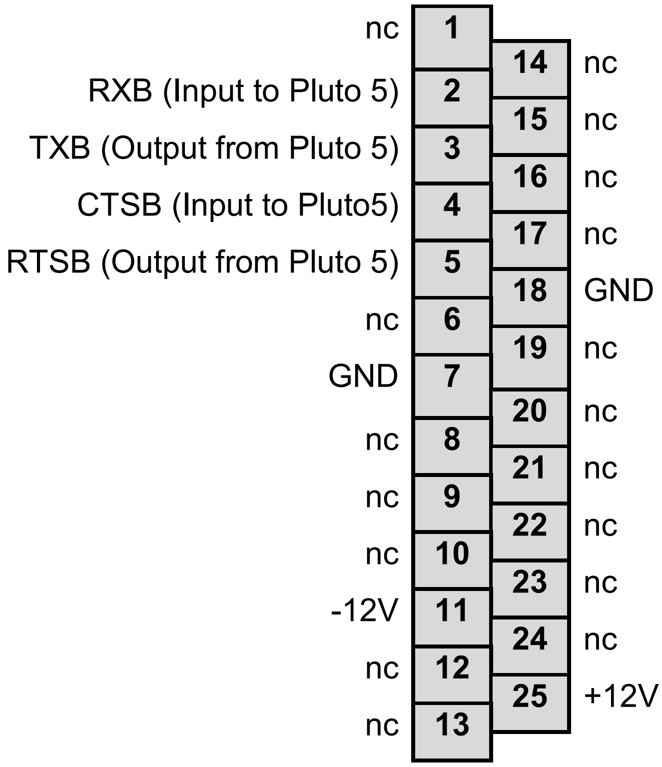
9.2 P1 – RS232 Channel A

Reference: P1
Type: Header 6W AMP MTA-100
Description: RS232 Channel A

1	GND	
2	RXA	Input to Pluto 5
3	TXA	Output from Pluto 5
4	CTSA	Input to Pluto 5
5	RTSA	Output from Pluto 5
6	+12V	

9.3 P2 – Dataport (RS232 Channel B)

Reference: P2
Type: 25W ‘D’ Socket
Description: BACTA Dataport / RS232 Channel B



9.4 P3 – Power Input

Reference: P3
Type: Header 6W AMP MTA-156
Description: Power

1	-12V	Neg supply for RS232 buffers
2	GND	Ground
3	GND	Ground
4	+12V	Main supply
5	GND	Ground
6	Vmpx+	Lamp MPX supply, +36V or +48V

9.5 P4 – Multiplexed Lamp Sinks

Reference: P4
Type: Header 18W AMP MTA-100
Description: Lamp Columns/Sinks

1	LC0	Lamp Column/Sink 0
2	LC1	Lamp Column/Sink 1
3	LC2	Lamp Column/Sink 2
4	LC3	Lamp Column/Sink 3
5	LC4	Lamp Column/Sink 4
6	LC5	Lamp Column/Sink 5
7	LC6	Lamp Column/Sink 6
8	LC7	Lamp Column/Sink 7
9	LC8	Lamp Column/Sink 8
10	LC9	Lamp Column/Sink 9
11	LC10	Lamp Column/Sink 10
12	LC11	Lamp Column/Sink 11
13	LC12	Lamp Column/Sink 12
14	LC13	Lamp Column/Sink 13
15	LC14	Lamp Column/Sink 14
16	LC15	Lamp Column/Sink 15
17	nc	No Connection
18	nc	No Connection

9.6 P5 Ultrex – Multiplexed LEDs

Reference: P5
Type: Header 32W AMP Ultrex
Description: LED - Drive for 16 or 32 seven-segment LED Digits.

Cathodes, Digit 0	DIG0	A1	B1	DIG1	Cathodes, Digit 1
Cathodes, Digit 2	DIG2	A2	B2	DIG3	Cathodes, Digit 3
Cathodes, Digit 4	DIG4	A3	B3	DIG5	Cathodes, Digit 5
Cathodes, Digit 6	DIG6	A4	B4	DIG7	Cathodes, Digit 7
Cathodes, Digit 8	DIG8	A5	B5	DIG9	Cathodes, Digit 9
Cathodes, Digit 10	DIG10	A6	B6	DIG11	Cathodes, Digit 11
Cathodes, Digit 12	DIG12	A7	B7	DIG13	Cathodes, Digit 13
Cathodes, Digit 14	DIG14	A8	B8	DIG15	Cathodes, Digit 15
Anodes, Segment 0	SEG0	A9	B9	SEG1	Anodes, Segment 1
Anodes, Segment 2	SEG2	A10	B10	SEG3	Anodes, Segment 3
Anodes, Segment 4	SEG4	A11	B11	SEG5	Anodes, Segment 5
Anodes, Segment 6	SEG6	A12	B12	SEG7	Anodes, Segment 7
Anodes, Segment 8	SEG8	A13	B13	SEG9	Anodes, Segment 9
Anodes, Segment 10	SEG10	A14	B14	SEG11	Anodes, Segment 11
Anodes, Segment 12	SEG12	A15	B15	SEG13	Anodes, Segment 13
Anodes, Segment 14	SEG14	A16	B16	SEG15	Anodes, Segment 15

9.7 P5 Box Header – Multiplexed LEDs

Reference: P5
Type: Header 34W Tyco Box Header
Description: LED - Drive for 16 or 32 seven-segment LED Digits.

Not Used		1	2	Not Used	
Cathodes, Digit 0	DIG0	3	4	DIG1	Cathodes, Digit 1
Cathodes, Digit 2	DIG2	5	6	DIG3	Cathodes, Digit 3
Cathodes, Digit 4	DIG4	7	8	DIG5	Cathodes, Digit 5
Cathodes, Digit 6	DIG6	9	10	DIG7	Cathodes, Digit 7
Cathodes, Digit 8	DIG8	11	12	DIG9	Cathodes, Digit 9
Cathodes, Digit 10	DIG10	13	14	DIG11	Cathodes, Digit 11
Cathodes, Digit 12	DIG12	15	16	DIG13	Cathodes, Digit 13
Cathodes, Digit 14	DIG14	17	18	DIG15	Cathodes, Digit 15
Anodes, Segment 0	SEG0	19	20	SEG1	Anodes, Segment 1
Anodes, Segment 2	SEG2	21	22	SEG3	Anodes, Segment 3
Anodes, Segment 4	SEG4	23	24	SEG5	Anodes, Segment 5
Anodes, Segment 6	SEG6	25	26	SEG7	Anodes, Segment 7
Anodes, Segment 8	SEG8	27	28	SEG9	Anodes, Segment 9
Anodes, Segment 10	SEG10	29	30	SEG11	Anodes, Segment 11
Anodes, Segment 12	SEG12	31	32	SEG13	Anodes, Segment 13
Anodes, Segment 14	SEG14	33	34	SEG15	Anodes, Segment 15

9.8 P6 – Multiplexed Lamps Sources

Reference: P6
Type: Header 16W AMP MTA-100
Description: Lamp Rows/Sources

1	LR0	Lamp Row/Source 0
2	LR1	Lamp Row/Source 1
3	LR2	Lamp Row/Source 2
4	LR3	Lamp Row/Source 3
5	LR4	Lamp Row/Source 4
6	LR5	Lamp Row/Source 5
7	LR6	Lamp Row/Source 6
8	LR7	Lamp Row/Source 7
9	LR8	Lamp Row/Source 8
10	LR9	Lamp Row/Source 9
11	LR10	Lamp Row/Source 10
12	LR11	Lamp Row/Source 11
13	LR12	Lamp Row/Source 12
14	LR13	Lamp Row/Source 13
15	LR14	Lamp Row/Source 14
16	LR15	Lamp Row/Source 15

9.9 P7 Ultrex – Reels

Reference: P7
Type: Header 50W AMP Ultrex
Description: Reels - Connector for 6 Stepper Motor Reel Mechanisms

Lamp Column 0	LC0	A1	B1	LC1	Lamp Column 1
Lamp Column 2	LC2	A2	B2	LC3	Lamp Column 3
Lamp Column 4	LC4	A3	B3	LC5	Lamp Column 5
Lamp Row 0	LR0	A4	B4	LR1	Lamp Row 1
Lamp Row 2	LR2	A5	B5	LR3	Lamp Row 3
Lamp Row 4	LR4	A6	B6	LR5	Lamp Row 5
	GND	A7	B7	VCC	
Open Drain Output 0	OP0	A8	B8	OP1	Open Drain Output 1
Open Drain Output 2	OP2	A9	B9	OP3	Open Drain Output 3
Open Drain Output 4	OP4	A10	B10	OP5	Open Drain Output 5
Open Drain Output 6	OP6	A11	B11	OP7	Open Drain Output 7
Open Drain Output 8	OP8	A12	B12	OP9	Open Drain Output 9
Open Drain Output 10	OP10	A13	B13	OP11	Open Drain Output 11
Open Drain Output 12	OP12	A14	B14	OP13	Open Drain Output 13
Open Drain Output 14	OP14	A15	B15	OP15	Open Drain Output 15
Open Drain Output 16	OP16	A16	B16	OP17	Open Drain Output 17
Open Drain Output 18	OP18	A17	B17	OP19	Open Drain Output 19
Open Drain Output 20	OP20	A18	B18	OP21	Open Drain Output 21
Open Drain Output 22	OP22	A19	B19	OP23	Open Drain Output 23
Input 0	IP0	A20	B20	IP1	Input 1
Input 2	IP2	A21	B21	IP3	Input 3
Input 4	IP4	A22	B22	IP5	Input 5
	+12V	A23	B23	+12V	
	+12V	A24	B24	+12V	
	+12V	A25	B25	+12V	

9.10 P7 Box Header – Reels

Reference: P7
Type: Header 50W Tyco Box Header
Description: Reels - Connector for 6 Stepper Motor Reel Mechanisms

Lamp Column 0	LC0	1	2	LC1	Lamp Column 1
Lamp Column 2	LC2	3	4	LC3	Lamp Column 3
Lamp Column 4	LC4	5	6	LC5	Lamp Column 5
Lamp Row 0	LR0	7	8	LR1	Lamp Row 1
Lamp Row 2	LR2	9	10	LR3	Lamp Row 3
Lamp Row 4	LR4	11	12	LR5	Lamp Row 5
	GND	13	14	VCC	
Open Drain Output 0	OP0	15	16	OP1	Open Drain Output 1
Open Drain Output 2	OP2	17	18	OP3	Open Drain Output 3
Open Drain Output 4	OP4	19	20	OP5	Open Drain Output 5
Open Drain Output 6	OP6	21	22	OP7	Open Drain Output 7
Open Drain Output 8	OP8	23	24	OP9	Open Drain Output 9
Open Drain Output 10	OP10	25	26	OP11	Open Drain Output 11
Open Drain Output 12	OP12	27	28	OP13	Open Drain Output 13
Open Drain Output 14	OP14	29	30	OP15	Open Drain Output 15
Open Drain Output 16	OP16	31	32	OP17	Open Drain Output 17
Open Drain Output 18	OP18	33	34	OP19	Open Drain Output 19
Open Drain Output 20	OP20	35	36	OP21	Open Drain Output 21
Open Drain Output 22	OP22	37	38	OP23	Open Drain Output 23
Input 0	IP0	39	40	IP1	Input 1
Input 2	IP2	41	42	IP3	Input 3
Input 4	IP4	43	44	IP5	Input 5
	+12V	45	46	+12V	
	+12V	47	48	+12V	
	+12V	49	50	+12V	

9.11 P8 Ultrex – General I/O #1

Reference: P8
Type: Header 40W AMP Ultrex
Description: General Purpose I/O #1

Open Drain Output 24	OP24	A1	B1	OP25	Open Drain Output 25
Open Drain Output 26	OP26	A2	B2	OP27	Open Drain Output 27
Open Drain Output 28	OP28	A3	B3	OP29	Open Drain Output 29
Open Drain Output 30	OP30	A4	B4	OP31	Open Drain Output 31
Open Drain Output 32	OP32	A5	B5	OP33	Open Drain Output 33
Open Drain Output 34	OP34	A6	B6	OP35	Open Drain Output 35
Open Drain Output 36	OP36	A7	B7	OP37	Open Drain Output 37
Open Drain Output 38	OP38	A8	B8	OP39	Open Drain Output 39
Open Drain Output 40	OP40	A9	B9	OP41	Open Drain Output 41
Open Drain Output 42	OP42	A10	B10	OP43	Open Drain Output 43
Open Drain Output 44	OP44	A11	B11	OP45	Open Drain Output 45
Open Drain Output 46	OP46	A12	B12	OP47	Open Drain Output 47
	GND	A13	B13	GND	
Input 20	IP20	A14	B14	IP21	Input 21
Input 22	IP22	A15	B15	IP23	Input 23
Input 24	IP24	A16	B16	IP25	Input 25
Input 26	IP26	A17	B17	IP27	Input 27
Input 28	IP28	A18	B18	IP29	Input 29
Input 30	IP30	A19	B19	IP31	Input 31
	+12V	A20	B20	+12V	

9.12 P8 Box Header – General I/O #1

Reference: P8
Type: Header 40W Tyco Box Header
Description: General Purpose I/O #1

Open Drain Output 24	OP24	1	2	OP25	Open Drain Output 25
Open Drain Output 26	OP26	3	4	OP27	Open Drain Output 27
Open Drain Output 28	OP28	5	6	OP29	Open Drain Output 29
Open Drain Output 30	OP30	7	8	OP31	Open Drain Output 31
Open Drain Output 32	OP32	9	10	OP33	Open Drain Output 33
Open Drain Output 34	OP34	11	12	OP35	Open Drain Output 35
Open Drain Output 36	OP36	13	14	OP37	Open Drain Output 37
Open Drain Output 38	OP38	15	16	OP39	Open Drain Output 39
Open Drain Output 40	OP40	17	18	OP41	Open Drain Output 41
Open Drain Output 42	OP42	19	20	OP43	Open Drain Output 43
Open Drain Output 44	OP44	21	22	OP45	Open Drain Output 45
Open Drain Output 46	OP46	23	24	OP47	Open Drain Output 47
	GND	25	26	GND	
Input 20	IP20	27	28	IP21	Input 21
Input 22	IP22	29	30	IP23	Input 23
Input 24	IP24	31	32	IP25	Input 25
Input 26	IP26	33	34	IP27	Input 27
Input 28	IP28	35	36	IP29	Input 29
Input 30	IP30	37	38	IP31	Input 31
	+12V	39	40	+12V	

9.13 P9 Ultrex – General I/O #2

Reference: P9
Type: Header 34W AMP Ultrex
Description: General Purpose I/O #2

Open drain Output 48	OP48	A1	B1	OP49	Open drain Output 49
Open drain Output 50	OP50	A2	B2	OP51	Open drain Output 51
Open drain Output 52	OP52	A3	B3	OP53	Open drain Output 53
Open drain Output 54	OP54	A4	B4	OP55	Open drain Output 55
Open drain Output 56	OP56	A5	B5	OP57	Open drain Output 57
Open drain Output 58	OP58	A6	B6	OP59	Open drain Output 59
Open drain Output 60	OP60	A7	B7	OP61	Open drain Output 61
Open drain Output 62	OP62	A8	B8	OP63	Open drain Output 63
	GND	A9	B9	GND	
Input 6	IP6	A10	B10	IP7	Input 7
Input 8	IP8	A11	B11	IP9	Input 9
Input 10	IP10	A12	B12	IP11	Input 11
Input 12	IP12	A13	B13	IP13	Input 13
Input 14	IP14	A14	B14	IP15	Input 15
Input 16	IP16	A15	B15	IP17	Input 17
Input 18	IP18	A16	B16	IP19	Input 19
	+12V	A17	B17	Vmeter	Current Sensing +12V

9.14 P9 Box Header – General I/O #2

Reference: P9
Type: Header 34W Box Header
Description: General Purpose I/O #2

Open drain Output 48	OP48	1	2	OP49	Open drain Output 49
Open drain Output 50	OP50	3	4	OP51	Open drain Output 51
Open drain Output 52	OP52	5	6	OP53	Open drain Output 53
Open drain Output 54	OP54	7	8	OP55	Open drain Output 55
Open drain Output 56	OP56	9	10	OP57	Open drain Output 57
Open drain Output 58	OP58	11	12	OP59	Open drain Output 59
Open drain Output 60	OP60	13	14	OP61	Open drain Output 61
Open drain Output 62	OP62	15	16	OP63	Open drain Output 63
	GND	17	18	GND	
Input 6	IP6	19	20	IP7	Input 7
Input 8	IP8	21	22	IP9	Input 9
Input 10	IP10	23	24	IP11	Input 11
Input 12	IP12	25	26	IP13	Input 13
Input 14	IP14	27	28	IP15	Input 15
Input 16	IP16	29	30	IP17	Input 17
Input 18	IP18	31	32	IP19	Input 19
	+12V	33	34	Vmeter	Current Sensing +12V

9.15 P10 – Loudspeakers

Reference: P10
Type: Header 5W AMP MTA-100
Description: Loudspeakers

1	LS1+	Loudspeaker, Channel 1
2	LS1-	Loudspeaker, Channel 1
3	MIX	Channel 2 mixer input
4	LS2+	Loudspeaker, Channel 2
5	LS2-	Loudspeaker, Channel 2

WARNING: Loudspeaker outputs are bridge driven and must **NOT** be connected ground.

9.16 P11 – Multiplex Expansion

Reference: P11
Type: Header 7W AMP MTA-100
Description: Multiplex Expansion

1	MPX1_DATA_A	12V CMOS Output
2	Logic "1" Level	12V CMOS Output
3	MPX_STR_A	12V CMOS Output
4	GND	
5	MPX_CLK	12V CMOS Output
6	MPX_STR	12V CMOS Output
7	MPX_OE	12V CMOS Output

9.17 P12 – Aux Outputs

Reference: P12
Type: Header 8W AMP MTA-100
Description: Aux. Outputs

1	GND	
2	AUX0	Open drain output, 150mA, 1K pull-up to +5V
3	AUX1	Open drain output, 150mA, 1K pull-up to +5V
4	AUX2	Open drain output, 150mA, 1K pull-up to +5V
5	AUX3	Open drain output, 150mA, 1K pull-up to +5V
6	AUX4	Open drain output, 150mA, 1K pull-up to +5V
7	AUX5	Open drain output, 150mA, 1K pull-up to +5V
8	+12V	

9.18 P13 – External I²C Bus

Reference: P13
Type: Header 4W AMP MTA-100
Description: External I²C Bus

Pin	Signal	Description
1	GND	
2	AUX7/SDA	I2C SDA line, TTL Open Collector I/O, 1K Pull-up
3	AUX6/SCL	I2C SCL line, TTL Open Collector I/O, 1K Pull-up
4	+5V	

9.19 P14 – IO Expansion Card Connector

Reference: P14
Type: DIN41612, C/2 Vertical Plug
Description: Connector for IO Expansion Boards

	c	*b*	*a*
1	D8	PORTA0	HALT-
2	D9	PORTA1	CLKOUT
3	D10	PORTA2	CS3-
4	D11	PORTA3	RESET-
5	D12	PORTA4	BERR-
6	D13	PORTA5	A20
7	D14	A22	A23
8	D15	AS-	A4
9	RXDA- (TTL)	DS-	A5
10	TXDA- (TTL)	R/W-	A6
11	CTSA- (TTL)	DSACK0-	A7
12	RTSA- (TTL)	DSACK1-	+12V
13	A0	SIZ0	VCC
14	A1	SIZ1	VCC
15	A2	PB5	GND
16	A3	PB6	GND

9.20 P15 – Memory Expansion Card Connector

Reference: P15
Type: DIN41612, C/2 Socket Vertical
Description: Connector for Memory Expansion Boards

	a	*b*	*c*
1	A4	A5	A6
2	VCC	A7	A8
3	VCC	A9	A10
4	A3	A11	A12
5	A2	A13	A14
6	A1	A15	A16
7	GND	A17	A18
8	GND	A19	A20*
9	FPGA0	A21	D15
10	FPGA1	D14	D13
11	FPGA2	D12	D11
12	FPGA3	D10	D9
13	FPGA4	D8	D7
14	FPGA5	D6	D5
15	FPGA6	D1	D3
16	D0	D2	D4

*** NB**. - Pin c8, "A20" is in fact the connection to Pin 1 (ROM_P1) of the 2 on-board EPROMs, U1 & U2, and is driven by the FPGA.
For all memory accesses, **excluding** those to the ROM/EPROM area mapped by CS0-, the FPGA routes A20 to this pin.
For all memory accesses to the ROM/EPROM area mapped by CS0-, the FPGA routes either Vcc, A19 or A20 to this pin, depending on the memory mode set in the FPGA.

See Section 6.6, "EPROM Sockets / EPROM Autoselect Feature", for further information.

9.21 P16 – Background Debug Mode Connector

Reference: P16
Type: 10W Low Profile Header
Description: Background Debug Mode Connector
Only fitted to Software Development Boards

DS-	1	2	BERR-
GND	3	4	BKPT
GND	5	6	FREEZE
RESET-	7	8	IFETCH
VCC	9	10	IPIPE

9.22 P17 – RS232 Channel C

Reference: P17
Type: 9W 'D' Plug
Description: RS232 Channel C

Signal	Pin	Pin	Signal
GND	5		
		9	nc
DTRC[(1)] (Output from Pluto)	4		
		8	CTSC (Input to Pluto)
TXC (Output from Pluto)	3		
		7	RTSC (Output from Pluto)
RXC (Input to Pluto)	2		
		6	DSRC (Input to Pluto)
CDC (Input to Pluto)	1		

Note (1) – This signal (DTRC) is commoned with RTSD

9.23 P18 - RS232 Channels D, E, F & G.

Reference: P5
Type: Header 26W, 2.54mm Low Profile
Description: Connections for RS232 Channels D-G

	+12V	1	2	+12V	
	+12V	3	4	+12V	
Input to Pluto	RXD	5	6	RTSD	Output from Pluto
Output from Pluto	TXD	7	8	CTSD	Input to Pluto
	GND	9	10	GND	
Input to Pluto	RXE	11	12	RTSE	Output from Pluto
Output from Pluto	TXE	13	14	CTSE	Input to Pluto
	GND	15	16	GND	
Input to Pluto	RXF	17	18	RTSF	Output from Pluto
Output from Pluto	TXF	19	20	CTSF	Input to Pluto
	GND	21	22	GND	
Input to Pluto	RXG	23	24	RTSG	Output from Pluto
Output from Pluto	TXG	25	26	CTSG	Input to Pluto

9.24 P19 – Channel H – TTL Serial Port

Reference: P19
Type: Header 20W, 2.54mm Low Profile
Description: TTL Level Serial Port, Channel H

Power Out (100mA Max)	+12V	1	2	GND
Output from Pluto	TXDH	3	4	GND
Input to Pluto	RXDH	5	6	GND
Output from Pluto	RTSH	7	8	GND
Input to Pluto	CTSH	9	10	GND
Output from Pluto	OP2	11	12	GND
Output from Pluto	OP3	13	14	GND
Input to Pluto	IP2	15	16	GND
Input to Pluto	IP3	17	18	GND
	GND	19	20	GND

9.25 P20 – Power-Off Security Monitor

Reference: P20
Type: Header 8W AMP MTA-100
Description: 7 Switch Inputs, monitored while Pluto powered off

1	PSW1
2	PSW2
3	PSW3
4	PSW4
5	PSW5
6	PSW6
7	PSW7
8	PSW_COMMON

Figure 1 – Schematic Sheet 1 - Root Sheet

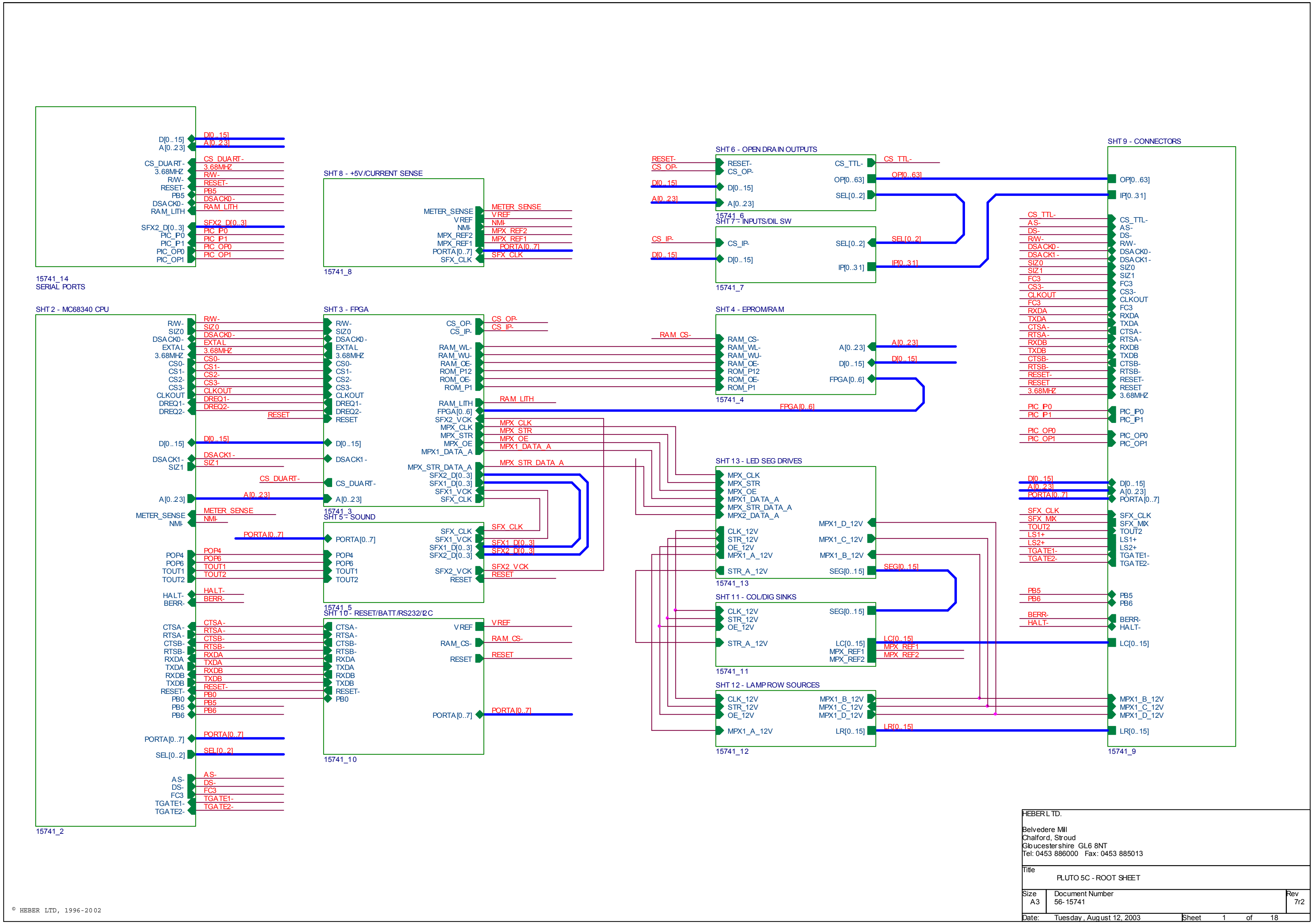


Figure 2 - Schematic Sheet 2 - CPU

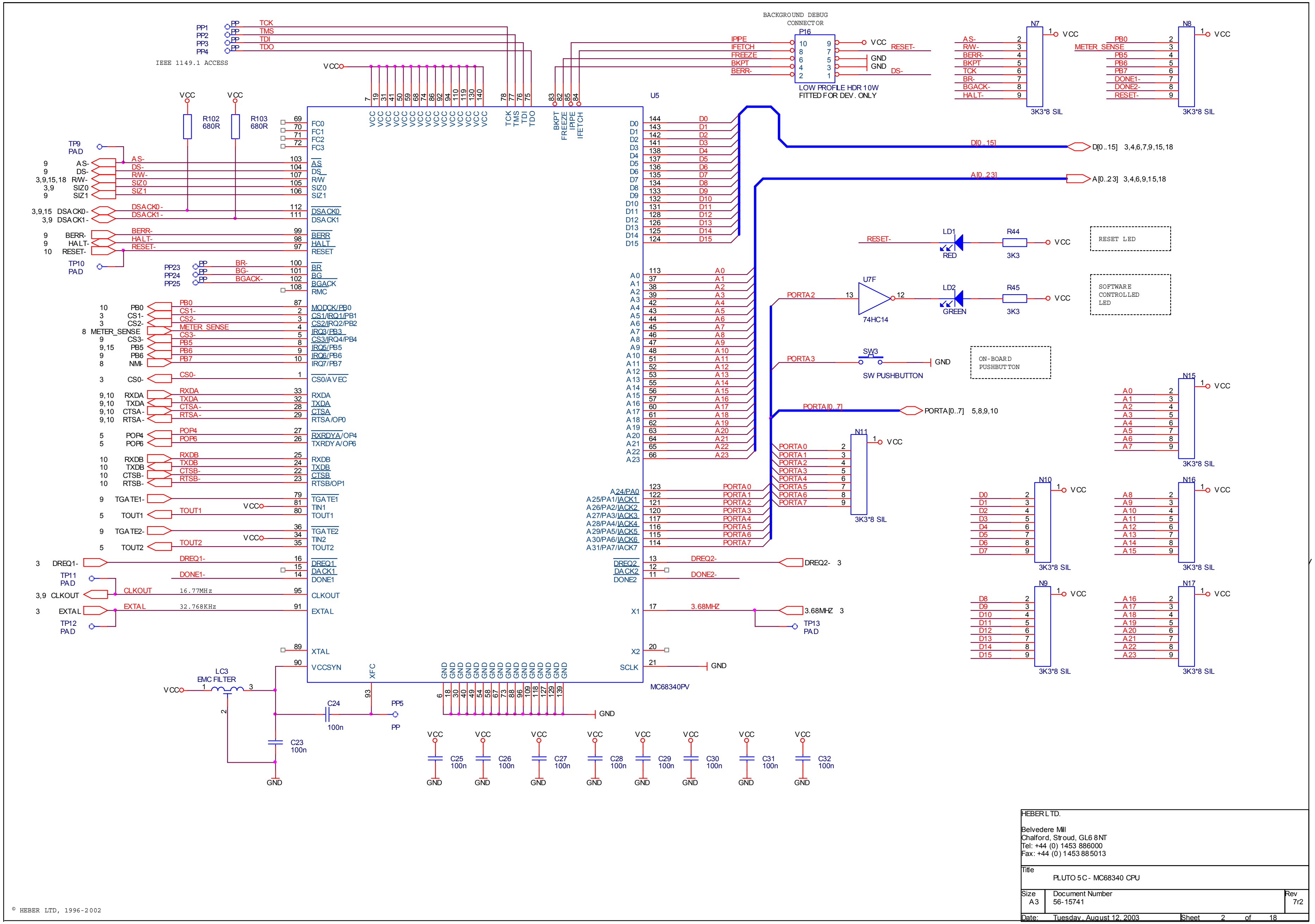


Figure 3 - Schematic Sheet 3 - FPGA

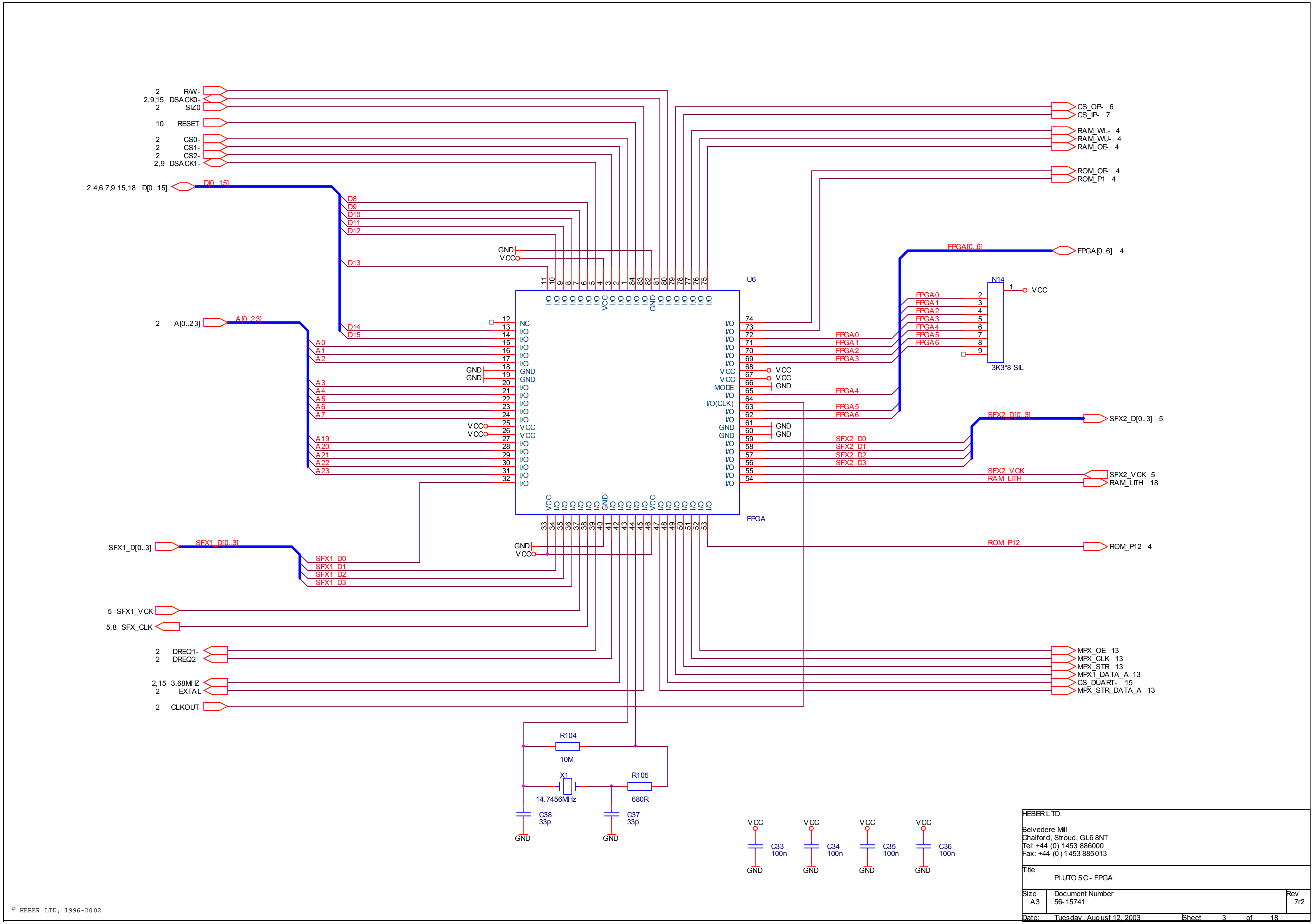
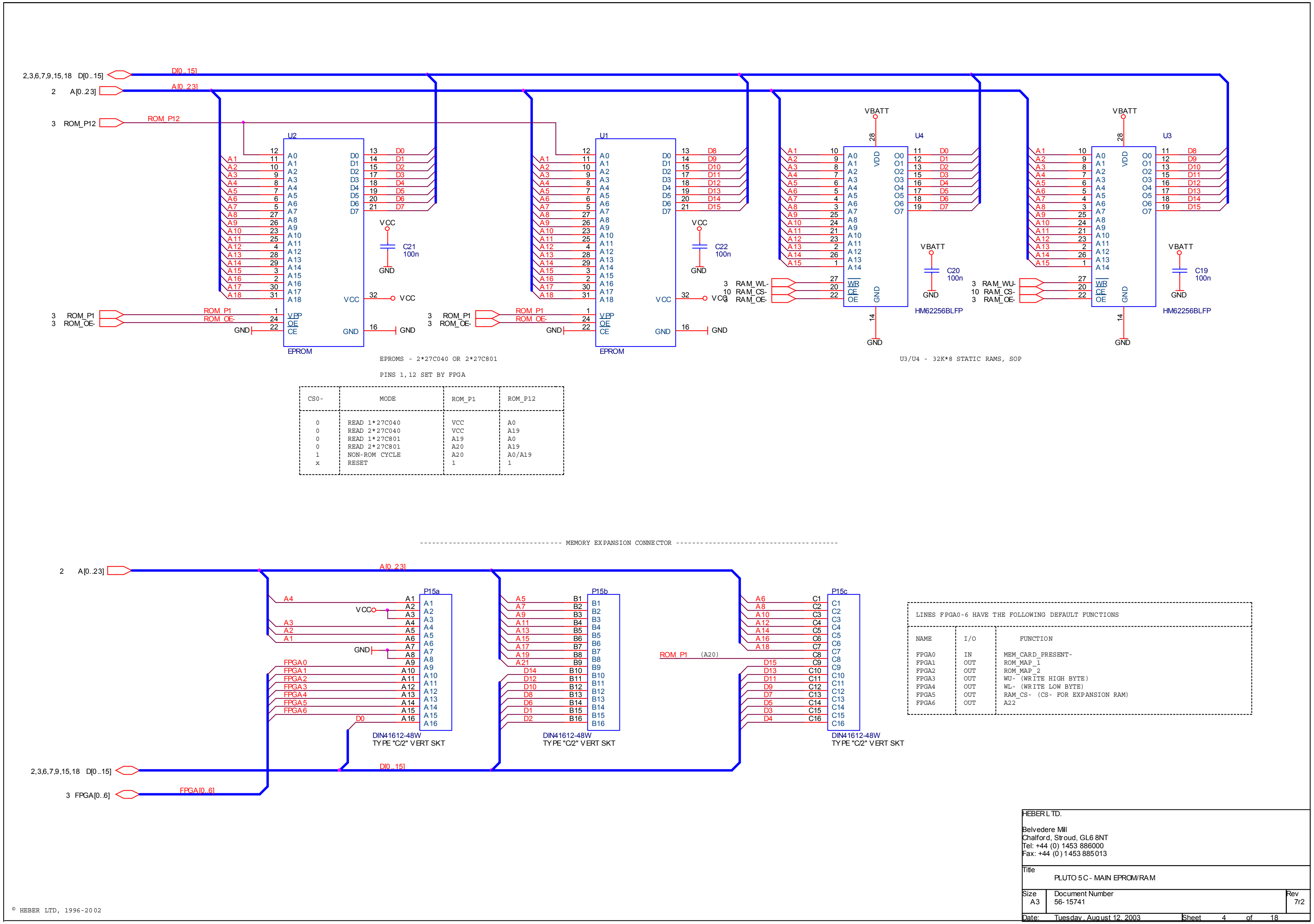


Figure 4 - Schematic Sheet 4 - Memory



CS0-	MODE	ROM_P1	ROM_P12
0	READ 1*27C040	VCC	A0
0	READ 2*27C040	VCC	A19
0	READ 1*27C801	A19	A0
0	READ 2*27C801	A20	A19
1	NON-ROM CYCLE	A20	A0/A19
x	RESET	1	1

LINES FPGA0-6 HAVE THE FOLLOWING DEFAULT FUNCTIONS

NAME	I/O	FUNCTION
FPGA0	IN	MEM_CARD_PRESENT-
FPGA1	OUT	ROM_MAP_1
FPGA2	OUT	ROM_MAP_2
FPGA3	OUT	WU- (WRITE HIGH BYTE)
FPGA4	OUT	WL- (WRITE LOW BYTE)
FPGA5	OUT	RAM_CS- (CS- FOR EXPANSION RAM)
FPGA6	OUT	A22

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Title	PLUTO 5C - MAIN EPROM/RAM	
Size A3	Document Number 56-15741	Rev 7r2
Date:	Tuesday, August 12, 2003	Sheet 4 of 18

Figure 5 - Schematic Sheet 5 - Sound

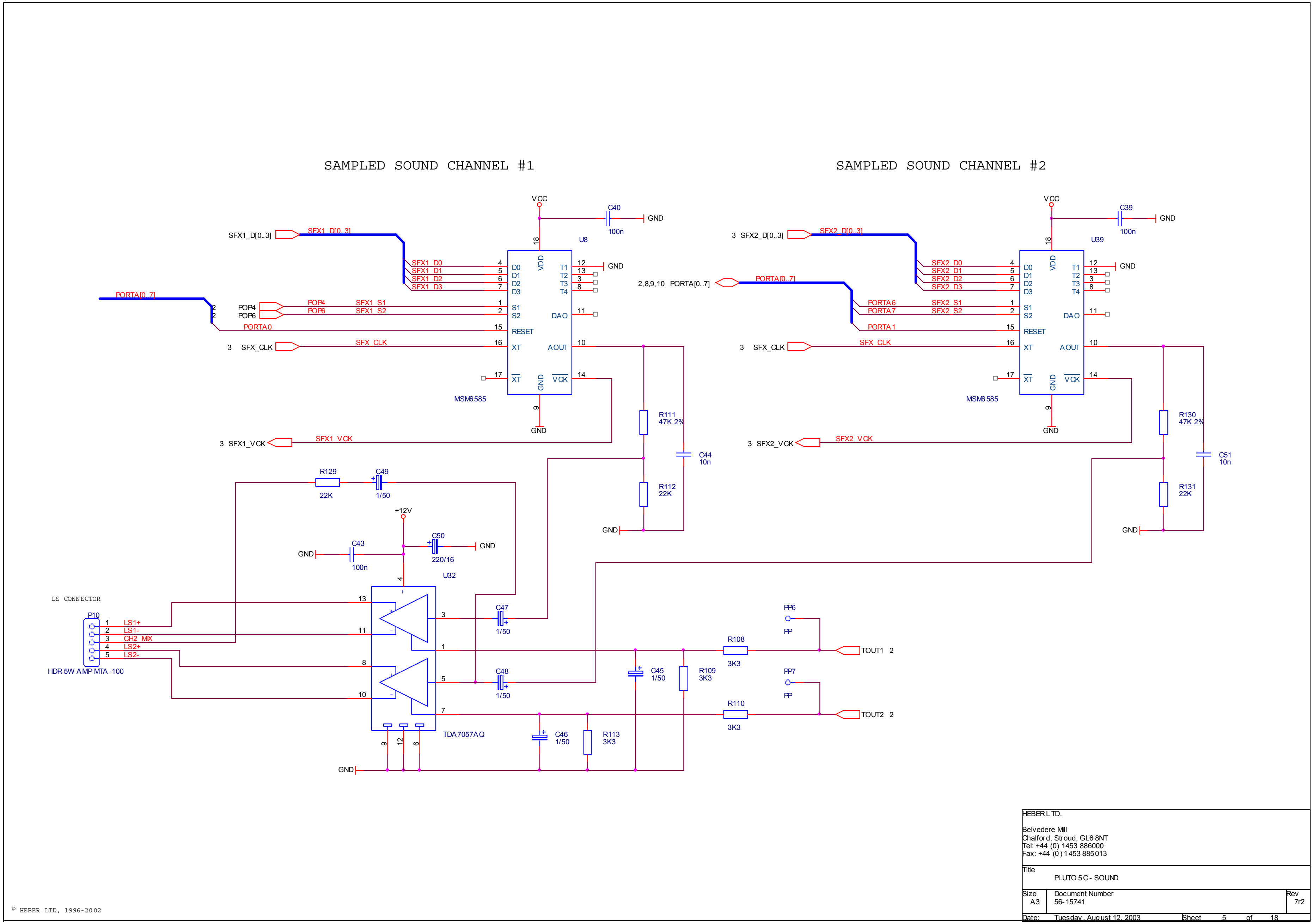


Figure 6 - Schematic Sheet 6 – Open Drain Outputs

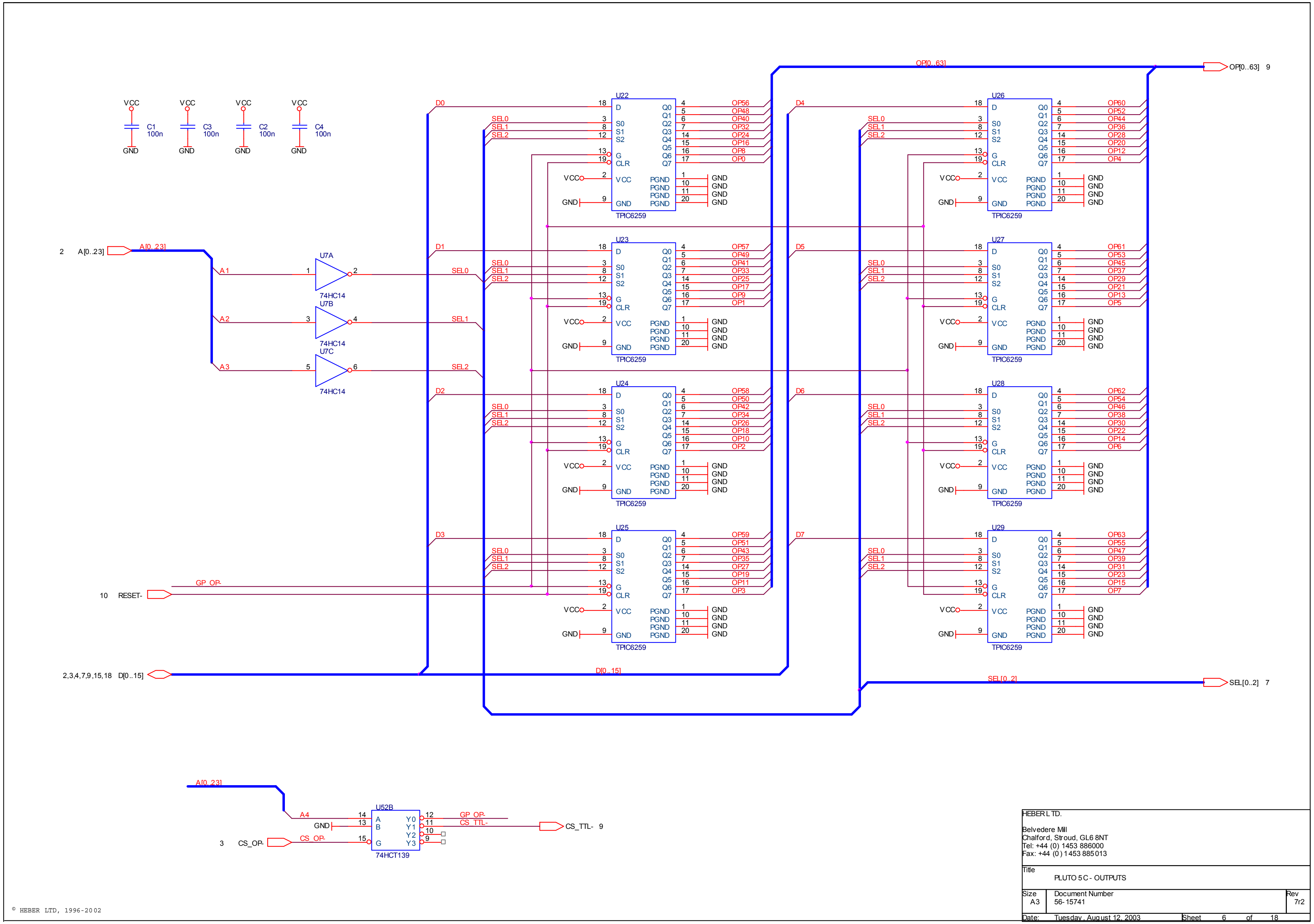


Figure 7 - Schematic Sheet 7 - Inputs

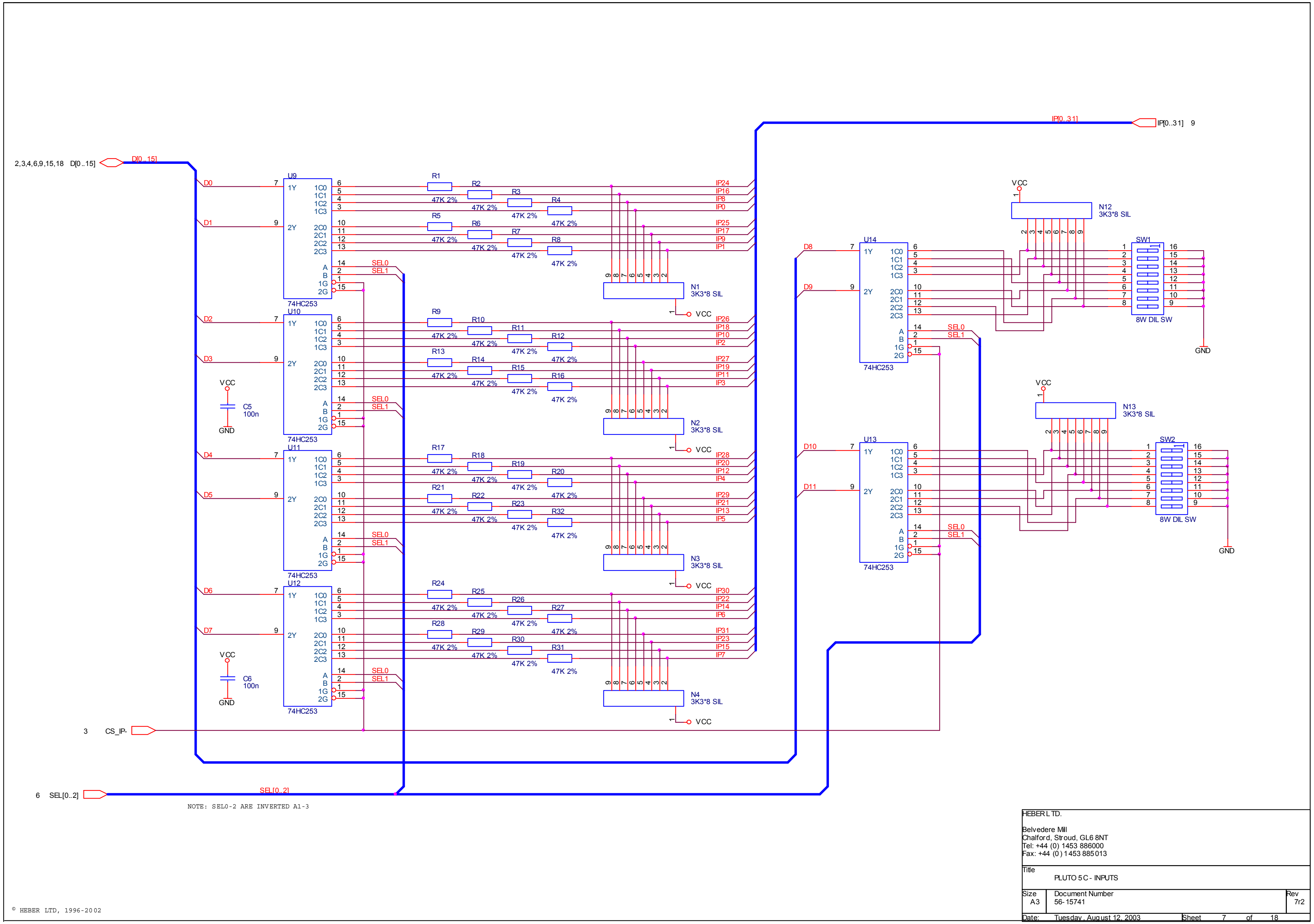


Figure 8 - Schematic Sheet 8 - Power Supply

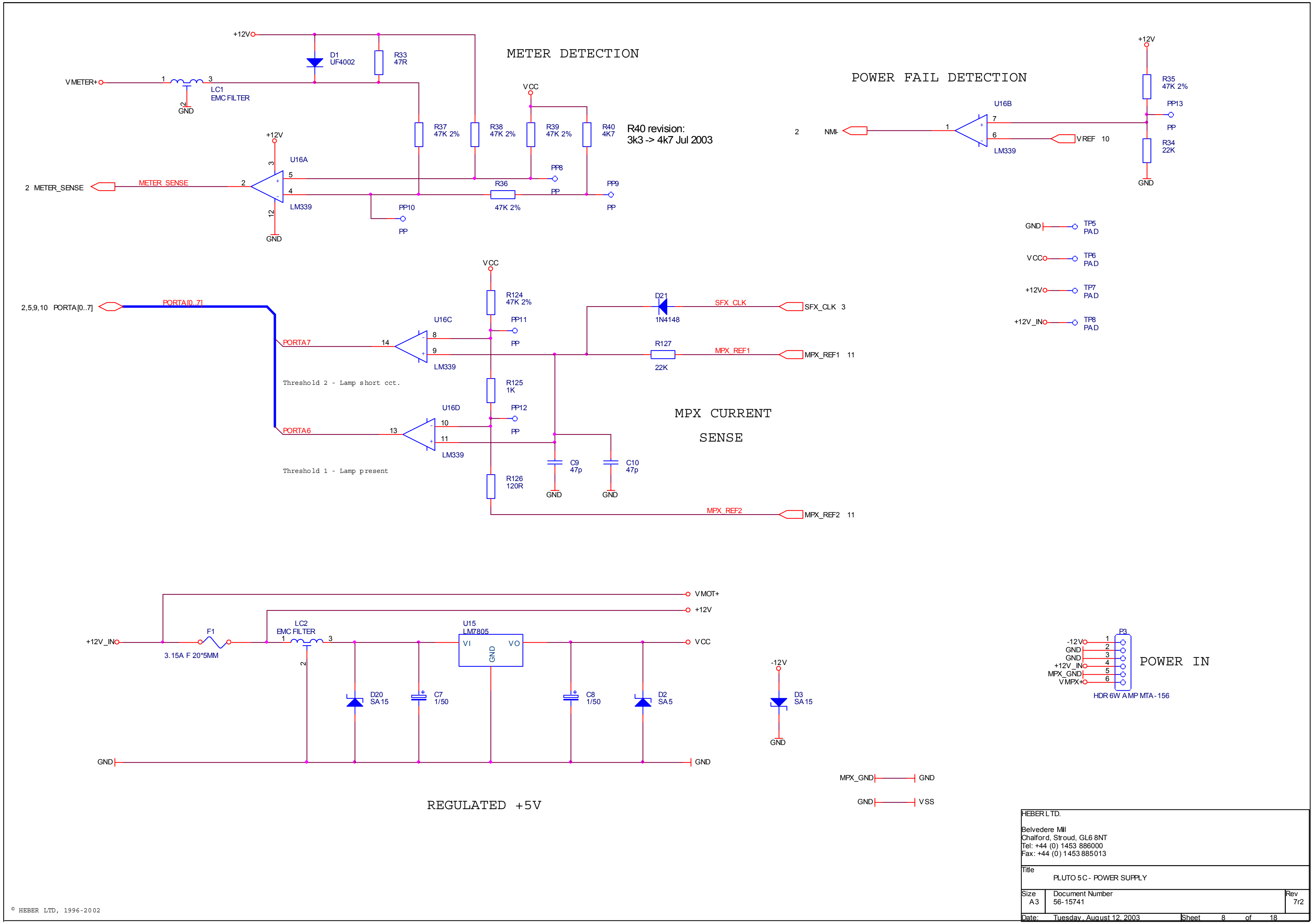


Figure 9 - Schematic Sheet 9 – IO Connectors

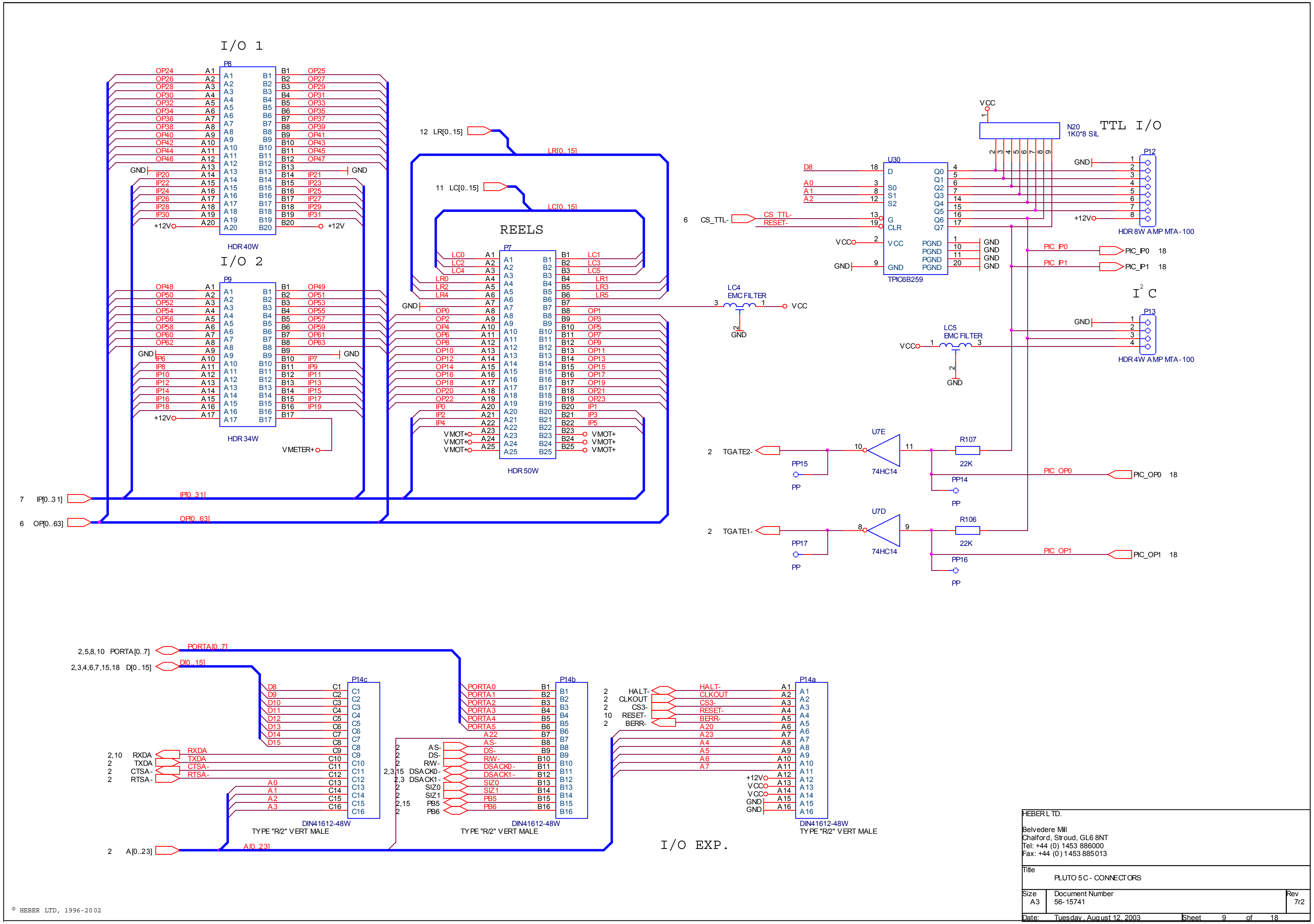


Figure 10 - Schematic Sheet 10 - Reset/Battery/RS232 Channels A & B

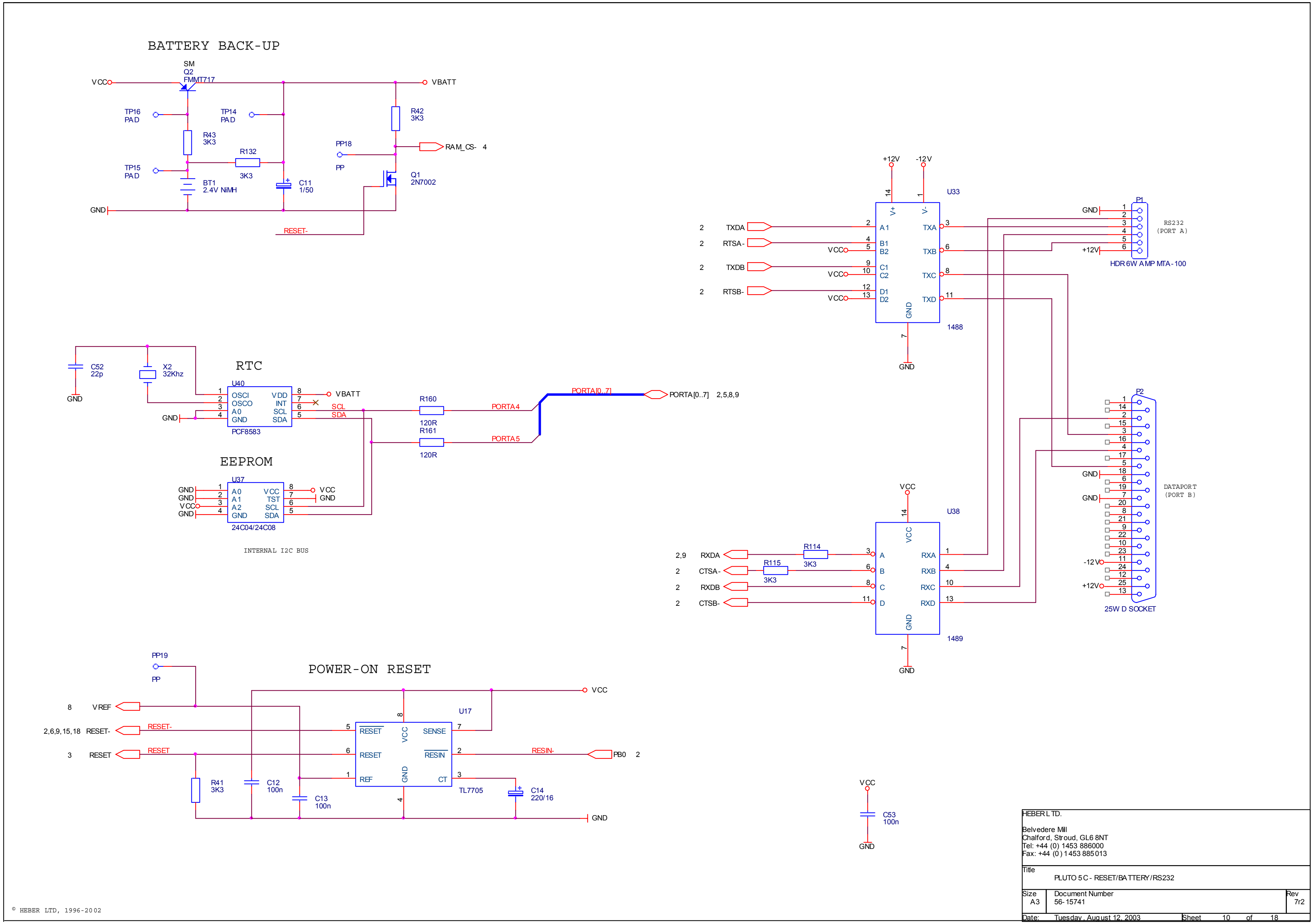


Figure 11- Schematic Sheet 11 - Lamp Column/LED Digit Drives

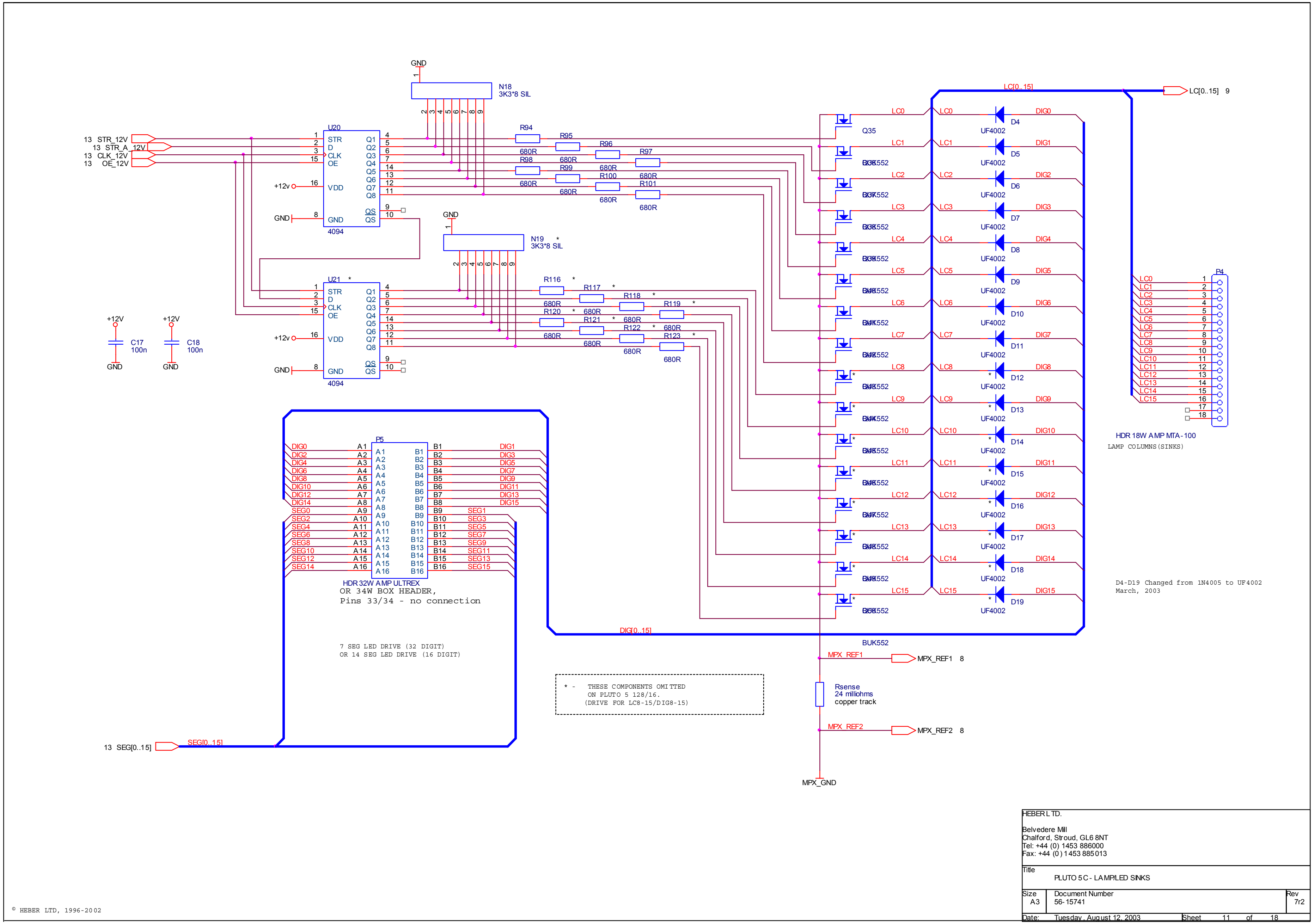


Figure 12 - Schematic Sheet 12 - Lamp Row Drives

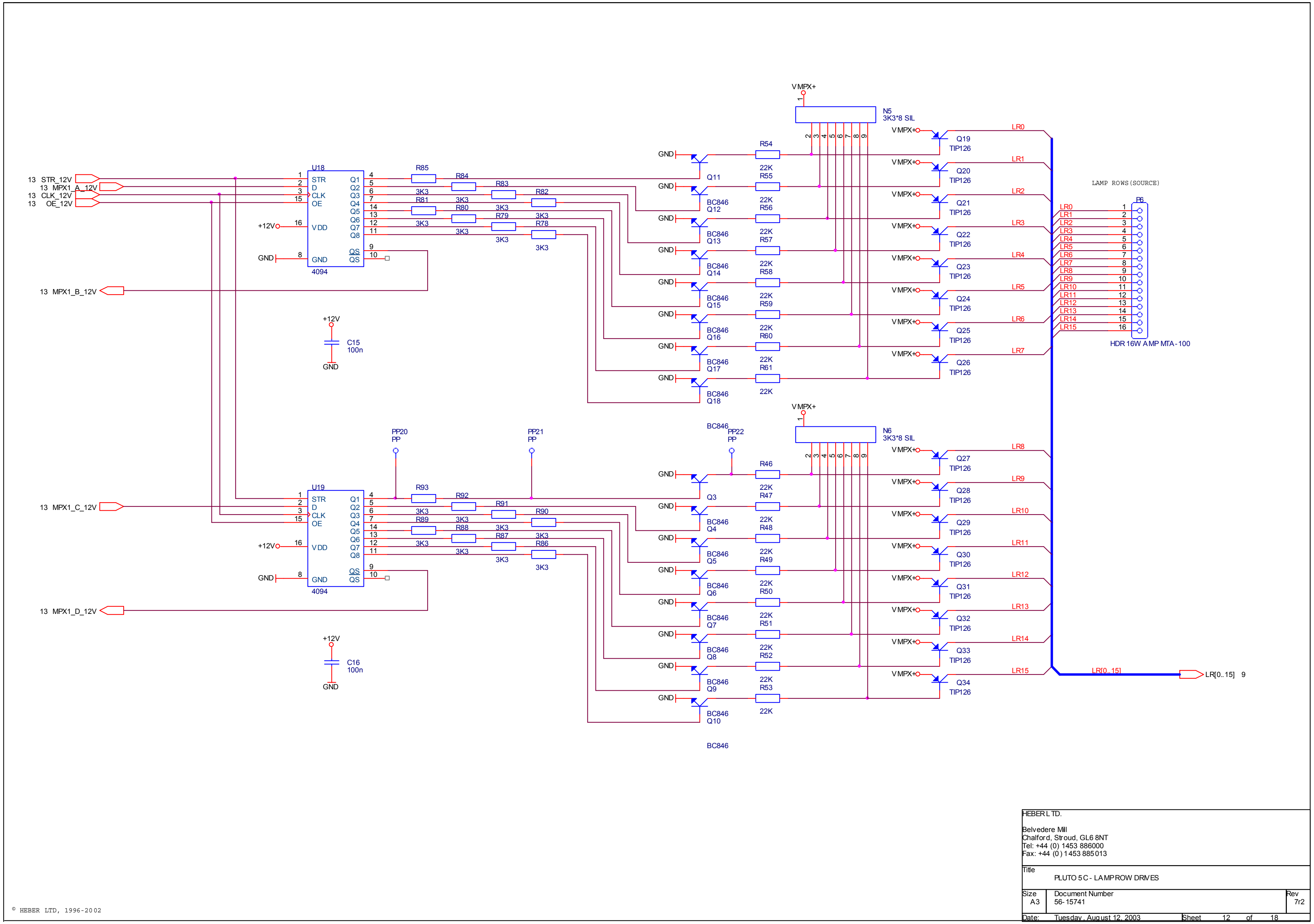


Figure 13 - Schematic Sheet 13 - LED Segment Drives

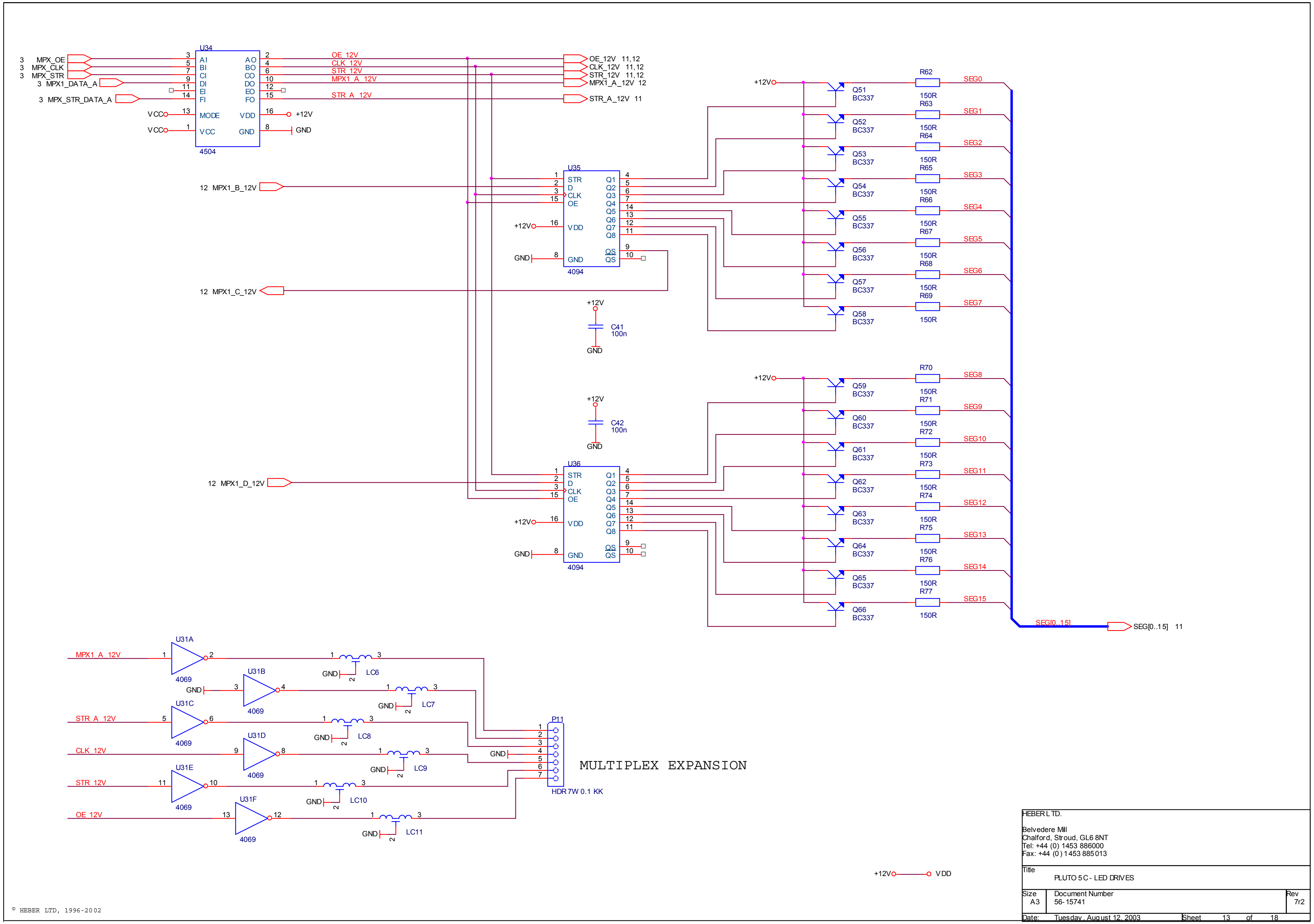


Figure 14 - Schematic Sheet 14 – Root Sheet 2

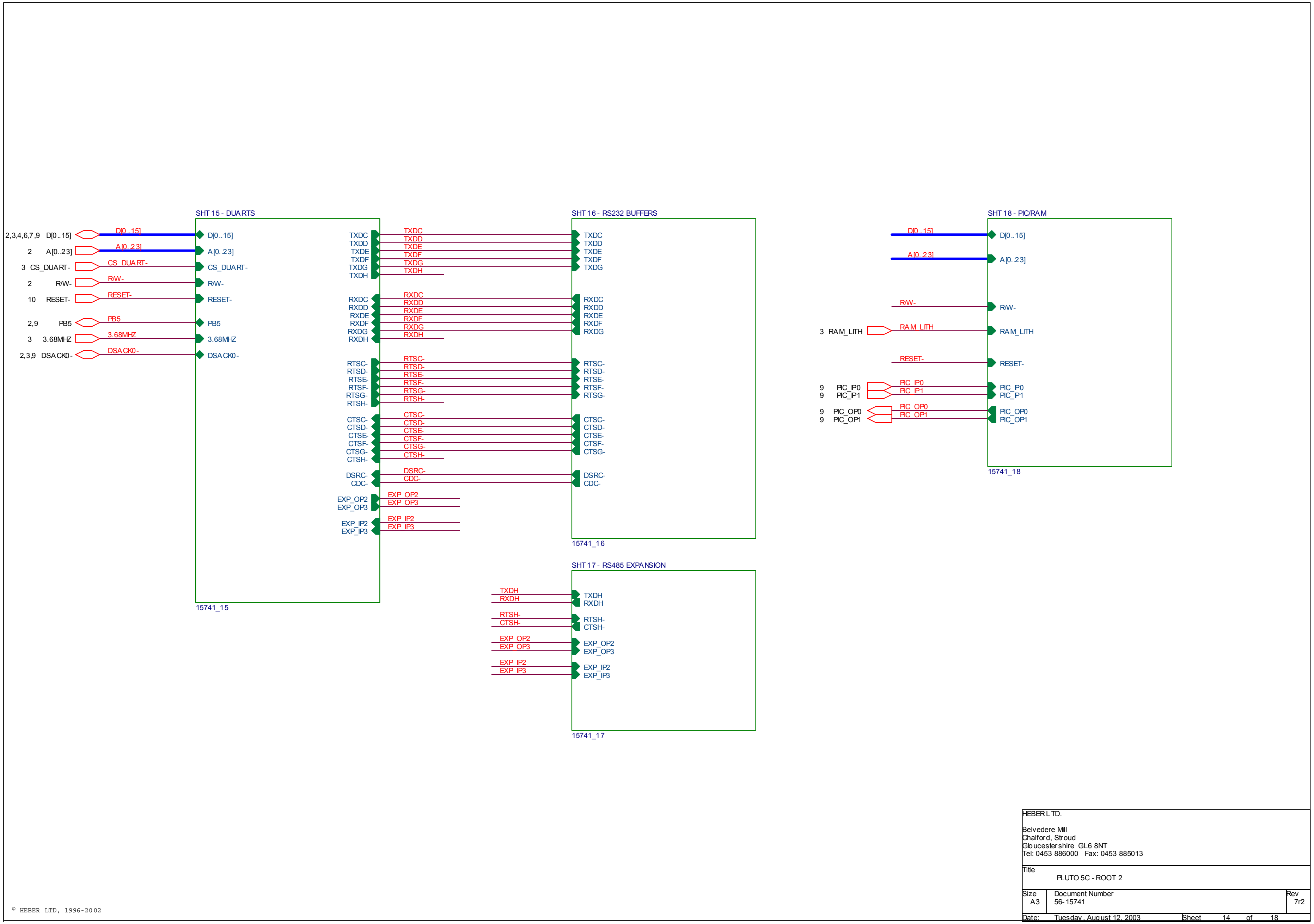


Figure 15 - Schematic Sheet 15 – DUARTS, Channels C-H

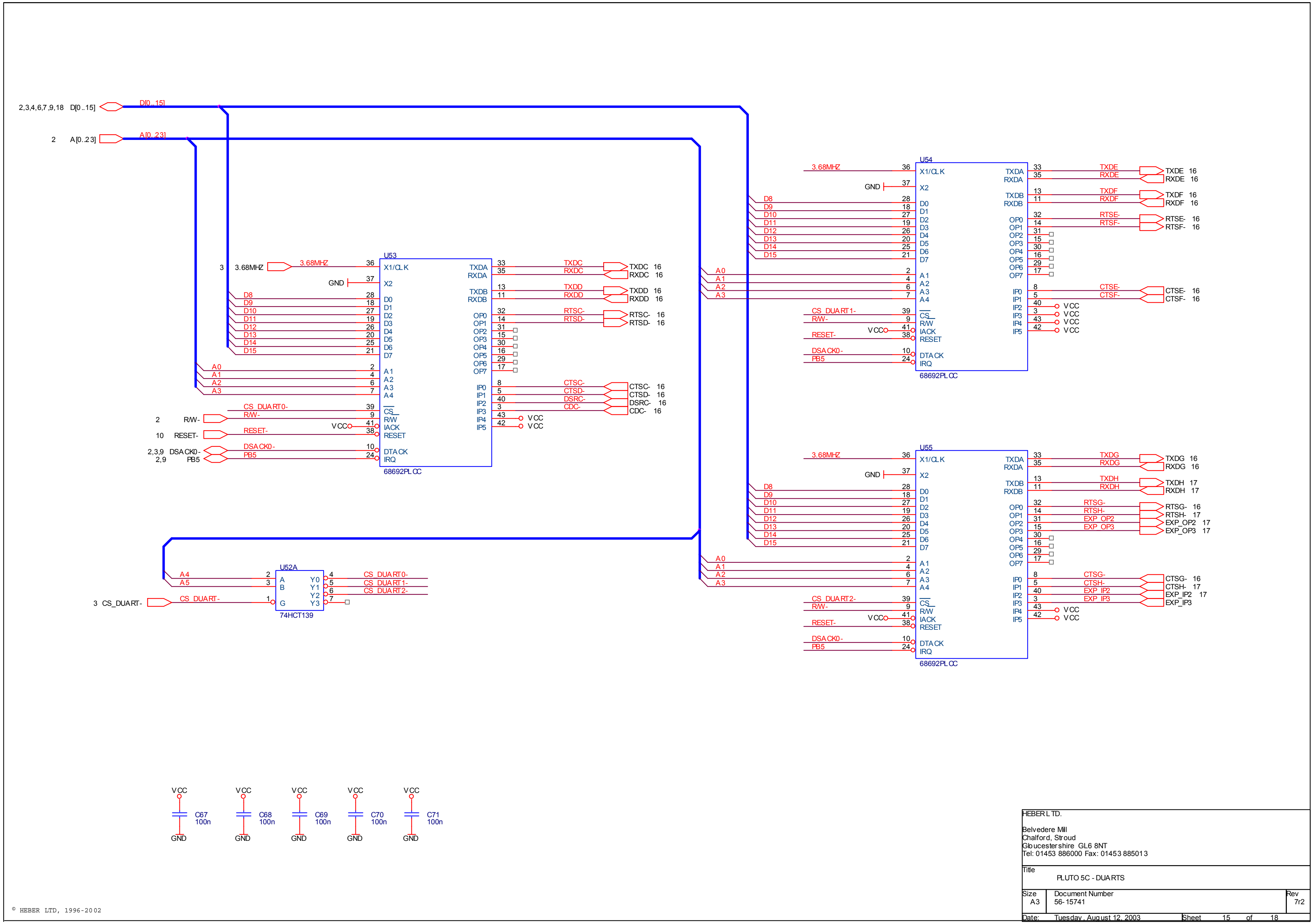


Figure 16 - Schematic Sheet 16 – RS232 Buffers Channels C-H

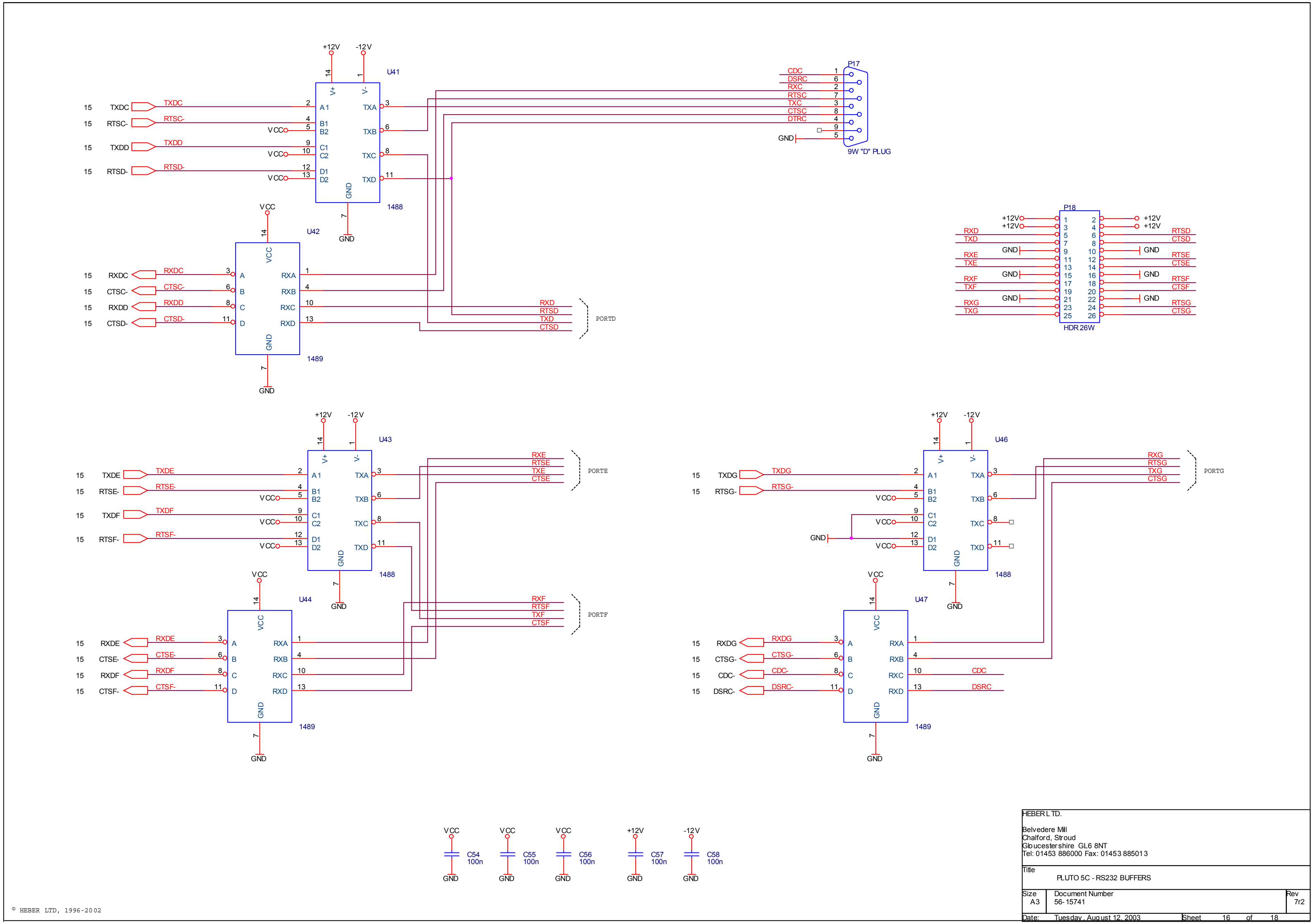


Figure 17 - Schematic Sheet 17 – Port H, TTL Buffers

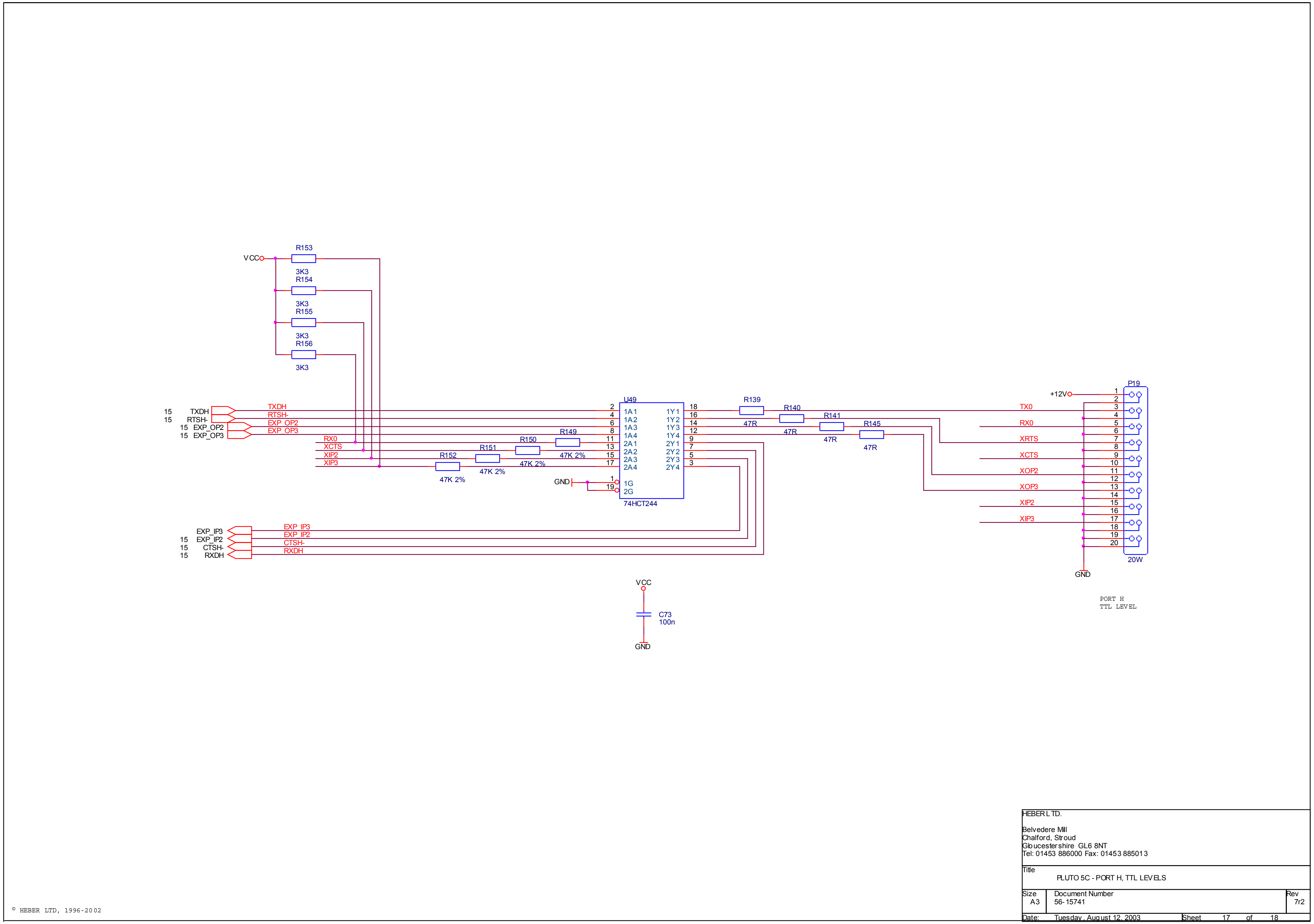


Figure 18 - Schematic Sheet 18 – Secondary NV RAM, Security PIC Microcontroller

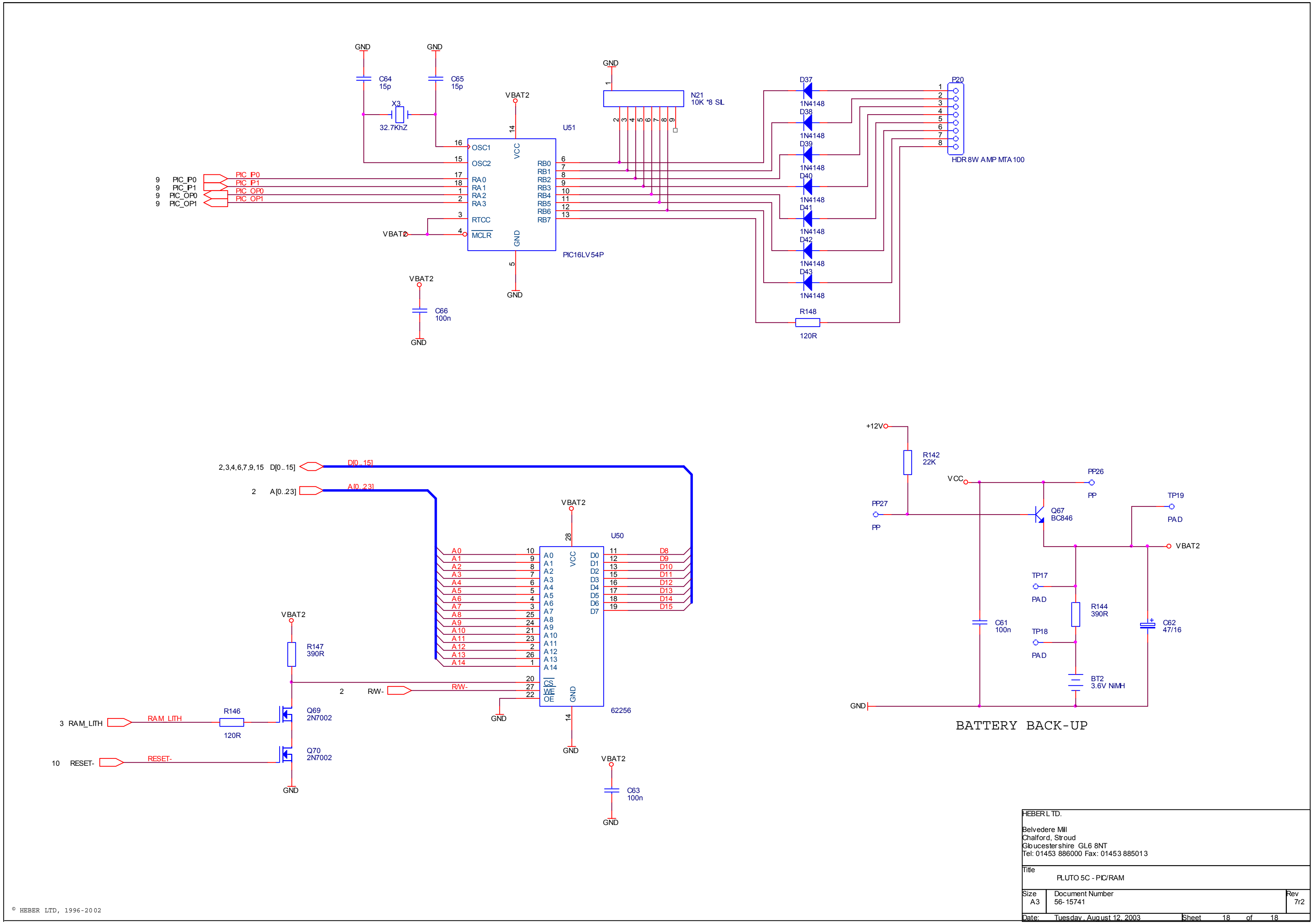


Figure 19 – Pluto 5 Casino with Ultrex connectors (Pluto 5CU) Photograph

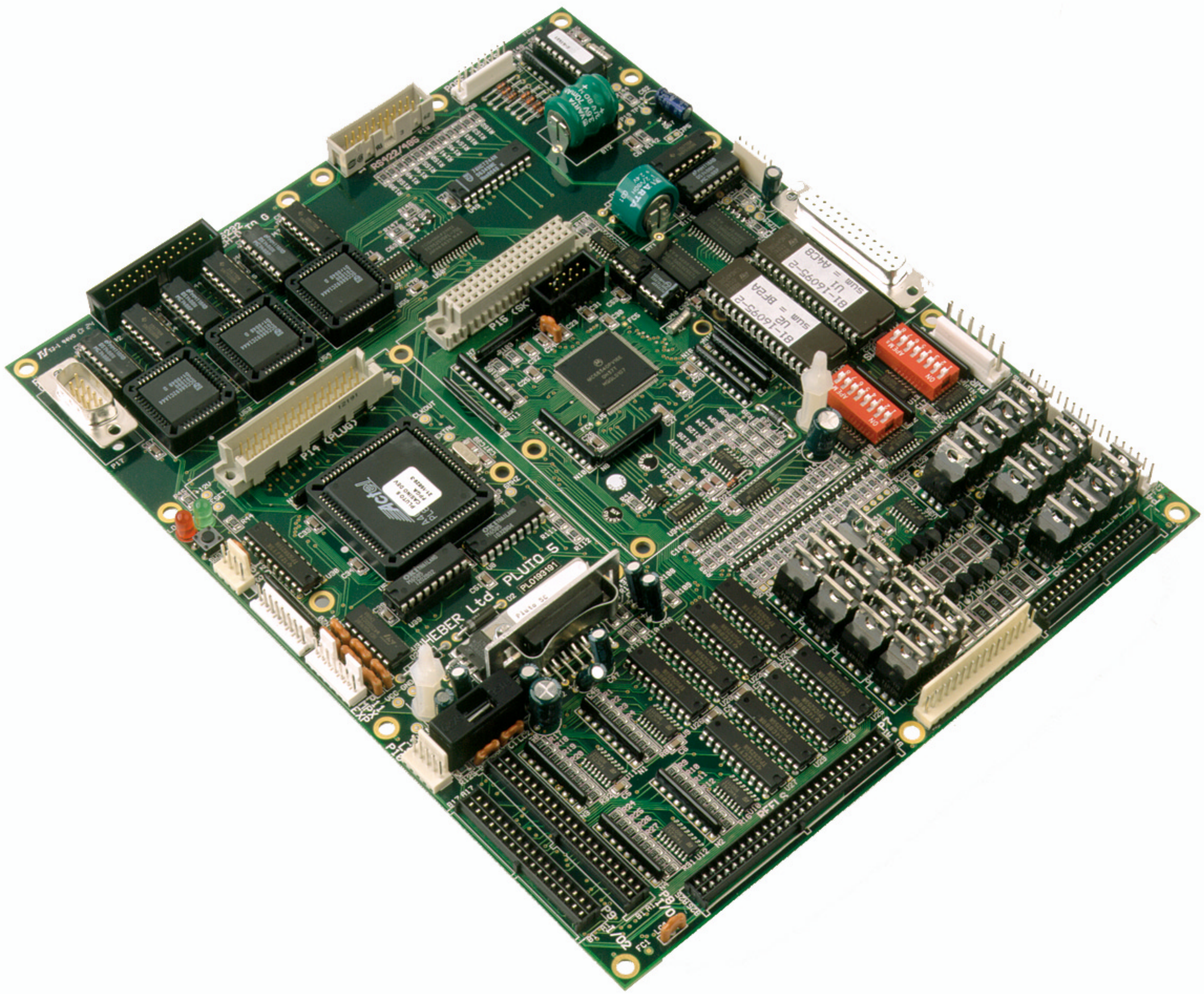


Figure 20 - Pluto 5 Casino Component Ident

